

1. General Description

The EM74LVC1GU04 is a single unbuffered inverter. Inputs can be driven from either 3.3 V or 5.5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

2. Features and Benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- Latch-up performance exceeds 100 mA
- ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 Class 3B exceeds 8000 V
 - MM JESD22-A115C Class C exceeds 550 V
 - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

EM74LVC1GU04

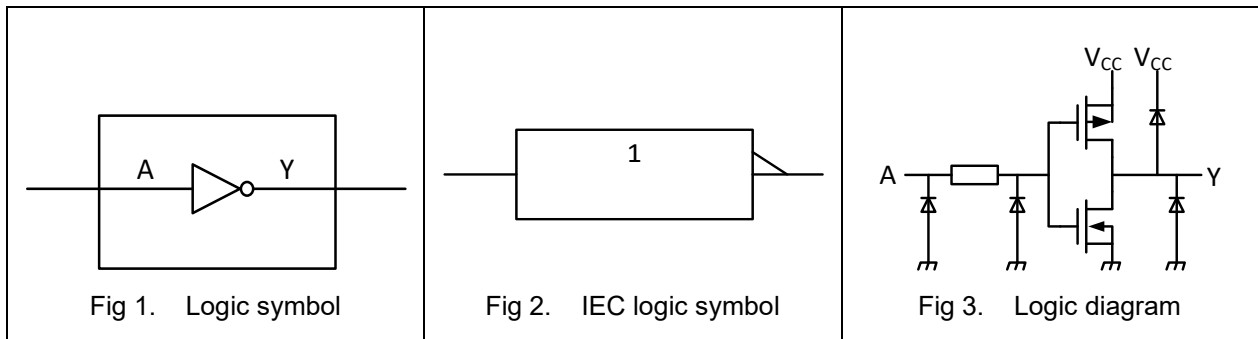
Unbuffered inverter

3. Ordering Information

Table 1. Ordering information

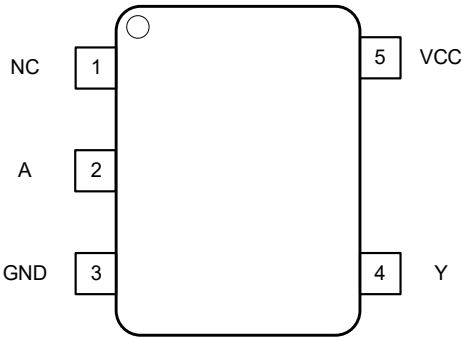
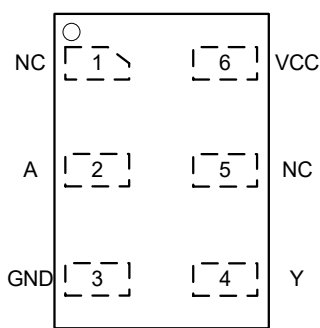
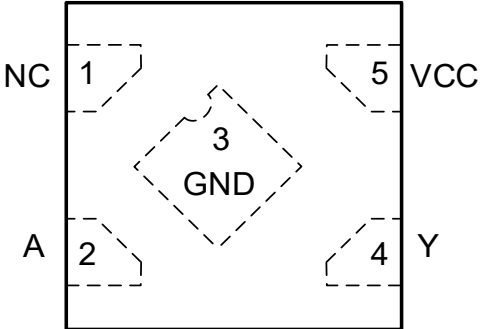
Type number	Topside marking	Package		Quantity
		Name	Description	
EM74LVC1GU04GV	VUYW	SOT23-5L	SOT23 package, 5 pins 2.92 mm × 1.6 mm; 1.25 mm (Max) height	3000
EM74LVC1GU04GW	VUYW	SOT353	SOT353 package, 5 pins 2.1 mm × 1.25 mm; 1.1 mm (Max) height	3000
EM74LVC1GU04GS	VU	DFN1x1-6L	DFN1×1 package, 6 pins 1 mm × 1 mm; 0.42 mm (Max) height	3000
EM74LVC1GU04GM	VUYW	DFN1x1.45-6L	DFN1.45×1 package, 6 pins 1.45 mm × 1 mm; 0.6 mm (Max) height	3000
EM74LVC1GU04GX	VU	DFN0.8x0.8-4L	DFN0.8×0.8 package, 5pins 0.8 mm × 0.8 mm; 0.4 mm (Max) height	3000

4. Function Diagram



5. Pinning Information

5.1. Pin map

 Fig 4. Top view pin configuration SOT23-5 and SOT353	 Fig 5. Top view pin configuration DFN6L
 Fig 6. Top view pin configuration DFN4L	

5.2. Pin description

Table 2. Pin description

Symbol	Pin		Description
	SOT23-5, SOT353 and DFN4L	DFN6L	
NC	1	1, 5	Not connected
A	2	2	Data input
GND	3	3	Ground (0V)
Y	4	4	Data output
VCC	5	6	Supply voltage