1. General Description

The EM74HC07; EM74HCT07 contains six buffers with open-drain outputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and Benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- High noise immunity
- CMOS low power dissipation
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- Input levels:
  - For EM74HC07: CMOS level
  - For EM74HCT07: TTL level
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 3500 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

3.Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
EM74HC07D	SOP-14L	plastic small outline package; 14 leads; body width 3.9 mm	3000
EM74HCT07D			
EM74HC07PW	TSSOP-14L	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	3000
EM74HCT07PW			

4.Function Diagram

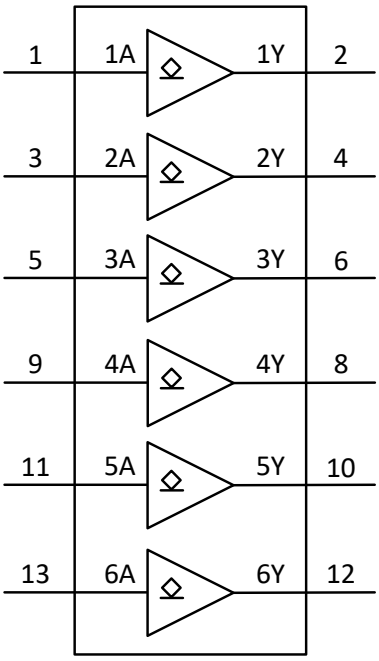

Fig. 1. Logic symbol

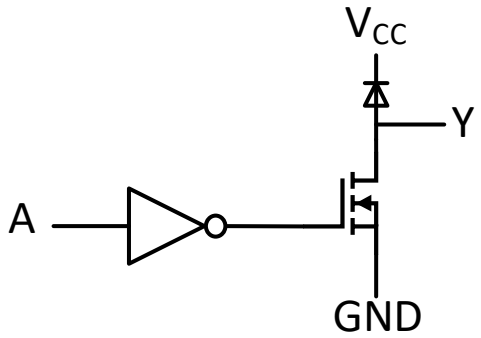

Fig. 2. Logic diagram(one gate)

5. Pinning Information

5.1. Pinning

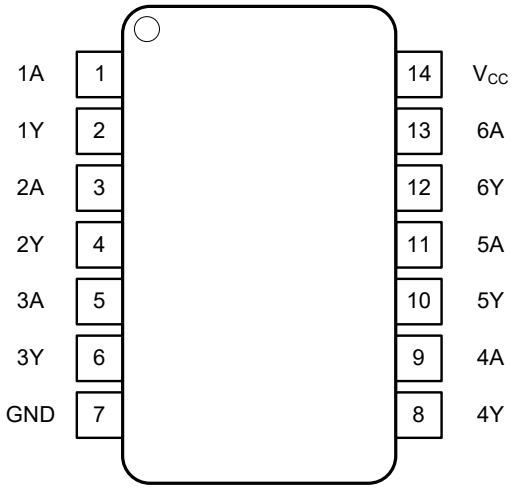

Fig. 3. Top view pin configuration SOP and TSSOP

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 6A	1, 3, 5, 9, 11, 13	Data input
1Y to 6Y	2, 4, 6, 8, 10, 12	Data output
GND	7	Ground (0V)
VCC	14	Supply voltage

6. Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	Output
nA	**nY**
L	L
H	Z