EM74LVC1G38

2-input NAND gate; open drain

Product datasheet, Rev1.0 Oct 30, 2023

1.General Description

The EM74LVC1G38 is a single 2-input NAND gate with open-drain output. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times. This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2.Features and Benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant outputs for interfacing with 5 V logic
- High noise immunity
- CMOS low power dissipation
- Open drain outputs
- Inputs accept voltages up to 5 V
- ±24 mA output drive (V_{CC} = 3.0 V)
- Latch-up performance exceeds 100 mA
- Direct interface with TTL levels
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 3B exceeds 8000 V
  - MM JESD22-A115C Class C exceeds 550 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

3.Ordering Information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Quantity
EM74LVC1G38GV	VGYW	SOT23-5L	SOT23 package, 5 pins 2.92 mm × 1.6 mm; 1.25 mm (Max) height	3000
EM74LVC1G38GW	VGYW	SOT353	SOT353 package, 5 pins 2.1 mm × 1.25 mm; 1.1 mm (Max) height	3000
EM74LVC1G38GS	VG	DFN1x1-6L	DFN1×1 package, 6 pins 1 mm × 1 mm; 0.42 mm (Max) height	3000
EM74LVC1G38GM	VGYW	DFN1x1.45-6L	DFN1.45×1 package, 6 pins 1.45 mm × 1 mm; 0.6 mm (Max) height	3000
EM74LVC1G38GX	VG	DFN0.8x0.8-4L	DFN0.8×0.8 package, 5pins 0.8 mm × 0.8 mm; 0.4 mm (Max) height	3000

4.Function Diagram

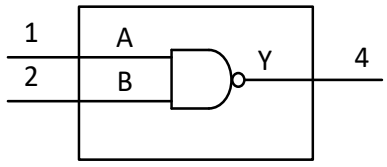


Fig 1. Logic symbol

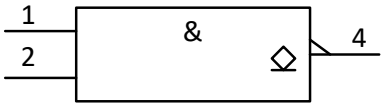


Fig 2. IEC logic symbol

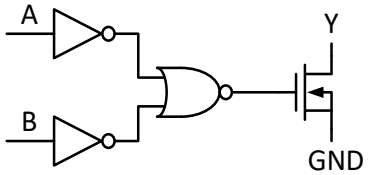


Fig 3. Logic diagram

5.Pinning Information

5.1. Pin map

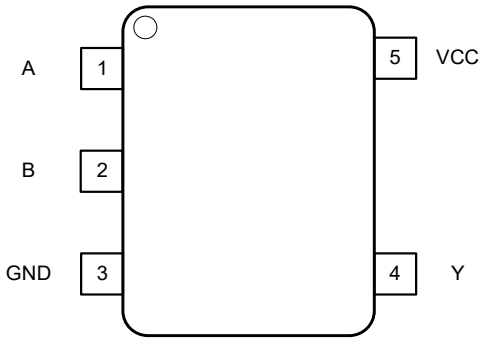


Fig 4. Top view pin configuration SOT23-5 and SOT353

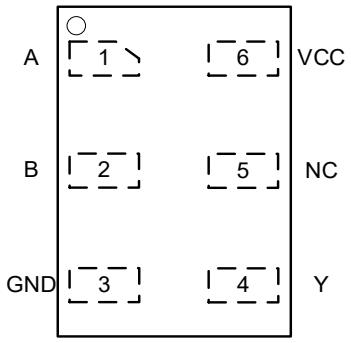


Fig 5. Top view pin configuration DFN6L

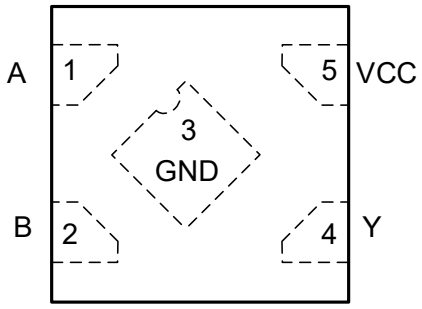


Fig 6. Top view pin configuration DFN4L

5.2. Pin description

Table 2. Pin description

Symbol	Pin		Description
	SOT23-5, SOT353 and DFN4L	DFN6L	
A	1	1,	Data input
B	2	2	Data input
GND	3	3	Ground (0V)
Y	4	4	Data output
NC	-	5	Not connected
VCC	5	6	Supply voltage

6.Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input		Output
A	**B**	**Y**
L	L	Z
L	H	Z
H	L	Z
H	H	L

7.Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50		mA
V_I	input voltage	[1]	-0.5	6.5	V
I_{OK}	output clamping current	$V_O < 0$ V	-50		mA
V_O	output voltage	Active mode [1]	-0.5	6.5	V
		Power-down mode; $V_{CC} = 0$ V [1]	-0.5	6.5	V
I_O	output current	V_O = 0 V to 6.5V		50	mA
I_{CC}	supply current			100	mA
I_{GND}	ground current		-100		mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to + 125 °C		250	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8.Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65		5.5	V
V_I	input voltage		0		5.5	V
V_O	output voltage	Active mode	0		5.5	V
		Power-down mode; V_{CC} = 0 V	0		5.5	V
T_{amb}	ambient temperature		-40		125	°C
$\Delta t/\Delta V$	Input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V			20	ns/V
		V_{CC} = 2.7 V to 5.5 V			10	ns/V

9.Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65V_{CC}			0.65V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7			1.7		V
		V_{CC} = 2.7 V to 3.6 V	2.0			2.0		V
		V_{CC} = 4.5 V to 5.5 V	0.7V_{CC}			0.7V_{CC}		V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V			0.35V_{CC}		0.35V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V			0.7		0.7	V
		V_{CC} = 2.7 V to 3.6 V			0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V			0.3V_{CC}		0.3V_{CC}	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100µA; V_{CC} = 1.65 V to 5.5 V			0.10		0.10	V
		I_O = 4 mA; V_{CC} = 1.65 V			0.45		0.70	V
		I_O = 8 mA; V_{CC} = 2.3 V			0.30		0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V			0.40		0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V			0.55		0.80	V
		I_O = 32 mA; V_{CC} = 4.5 V			0.55		0.80	V
I_I	Input leakage current	V_I = 5.5 V or GND ; V_{CC} = 0 V to 5.5 V		±0.1	±1		±1	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 5.5 V		±0.1	±2		±2	µA
I_{OFF}	power-off leakage current	V_{CC} = 0V ; V_I or V_O = 5.5 V		±0.1	±2		±2	µA
I_{CC}	supply current	V_I = 5.5V or GND ; I_O = 0A ; V_{CC} = 1.65V to 5.5V		0.1	4		4	µA
ΔI_{CC}	additional supply current	per pin ; V_{CC} = 2.3V to 5.5V ; V_I = V_{CC} -0.6V ; I_O = 0A		5	500		500	µA
C_I	input capacitance	V_{CC} = 3.3V ; V_I = GND to V_{CC}		5				pF

[1]All typical values are measured at V_{CC} = 3.3V and T_{amb} = 25℃.

10. Dynamic Characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	A to Y; see Fig. 7 [2]						
		V_{CC} = 1.65 V to 1.95 V	3.4	9.4	15.9	3.4	16.3	ns
		V_{CC} = 2.3 V to 2.7 V	2.4	5.0	8.6	2.4	9.1	ns
		V_{CC} = 3.0 V to 3.6 V	1.8	3.9	6.0	1.8	6.3	ns
		V_{CC} = 4.5 V to 5.5 V	1.4	2.6	3.6	1.4	3.8	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} ; V_{CC} = 3.3V [3]		3.5				pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

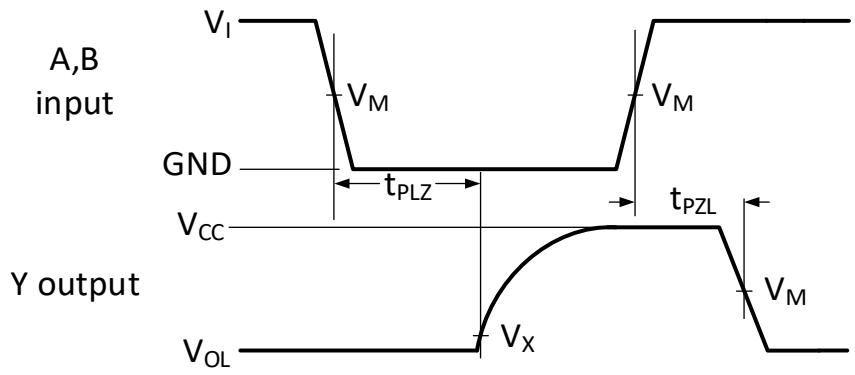
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit

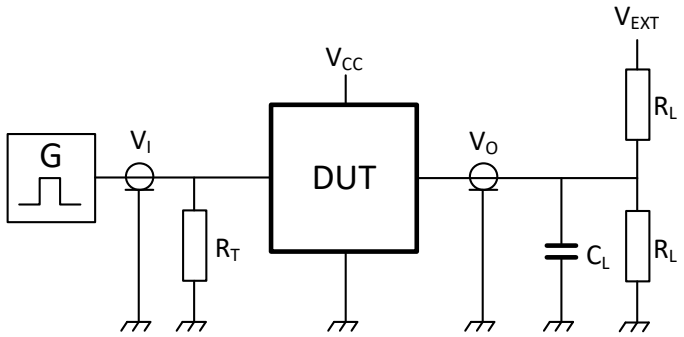


Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. The input A,B to output Y propagation delays

Table 8. Measurement points

Supply voltage	Input	Output	
V_{CC}	V_M	V_M	V_X
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15V
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15V
3.0 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3V
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.3V



Test data is given in Table 9.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
V_{EXT} = External voltage for measuring switching times.

Fig 8. Test circuit for measuring switching times

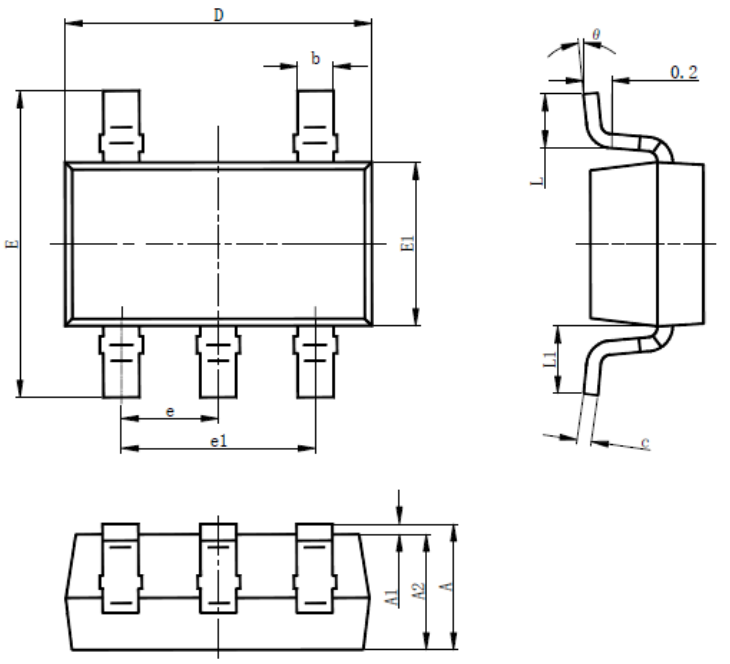
Table 9. Test data

Supply voltage	**Input**		**Load**		**V_{EXT}**
V_{CC}	**V_I**	**$t_r = t_f$**	**C_L**	**R_L**	**t_{PZL}, t_{PLZ}**
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	V_{CC}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	V_{CC}
3.0 V to 3.6 V	3 V	≤ 2.5 ns	50 pF	500 Ω	V_{CC}
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	V_{CC}

11. Package Outline

SOT23-5L

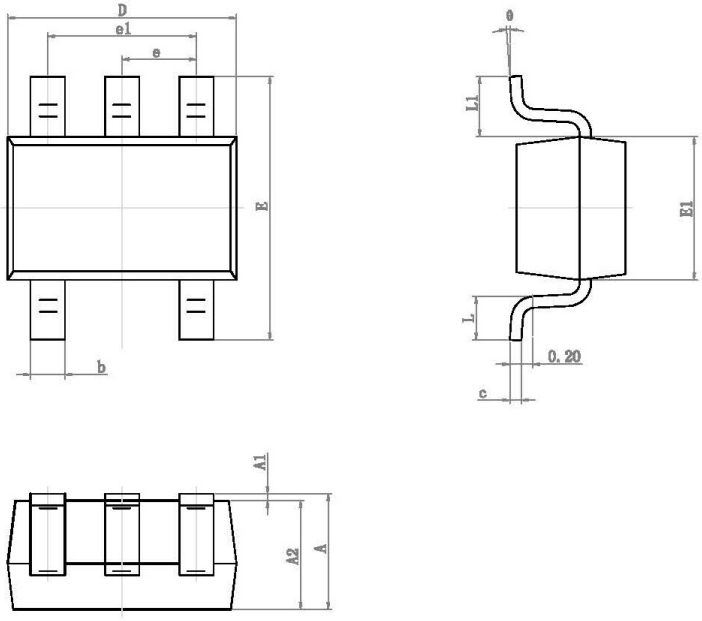
SOT-23-5L(14RZ) PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600REF.		0.024REF.	
θ	0°	8°	0°	8°

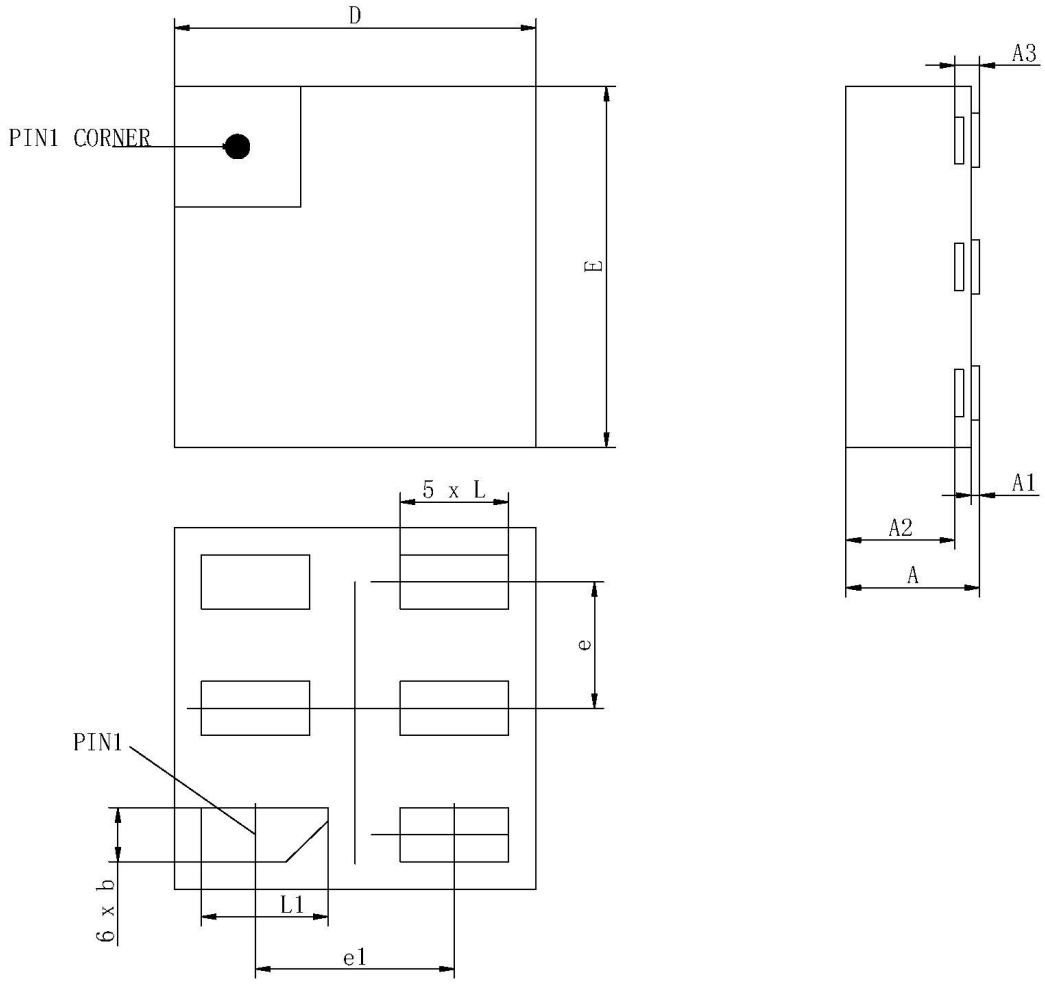
SOT353

SOT-353(16R) PACKAGE OUTLINE DIMENSIONS



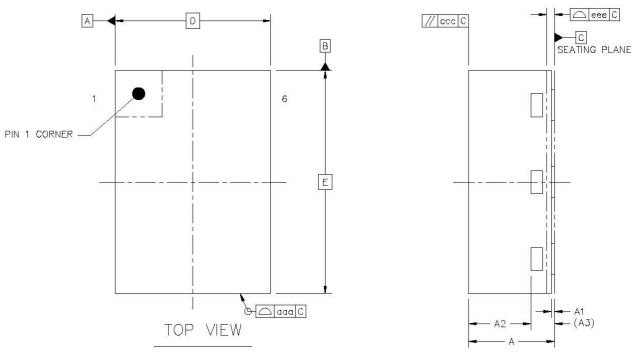
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.175	0.004	0.007
D	2.000	2.200	0.079	0.087
E	2.150	2.450	0.085	0.096
E1	1.150	1.350	0.045	0.053
e	0.650 TYP.		0.026 TYP.	
e1	1.200	1.400	0.047	0.055
L	0.260	0.460	0.010	0.018
L1	0.525 REF.		0.021 REF.	
θ	0°	8°	0°	8°

DFN1x1-6L



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.32	0.37	0.42
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.27	---
L/F THICKNESS		A3	0.102 REF		
BODY SIZE	X	D	1.00 BSC		
	Y	E	1.00 BSC		
LEAD WIDTH		b	0.10	0.15	0.20
LEAD PITCH		e	0.35 BSC		
		e1	0.55 BSC		
LEAD LENGTH		L	0.25	0.30	0.35
		L1	0.30	0.35	0.40

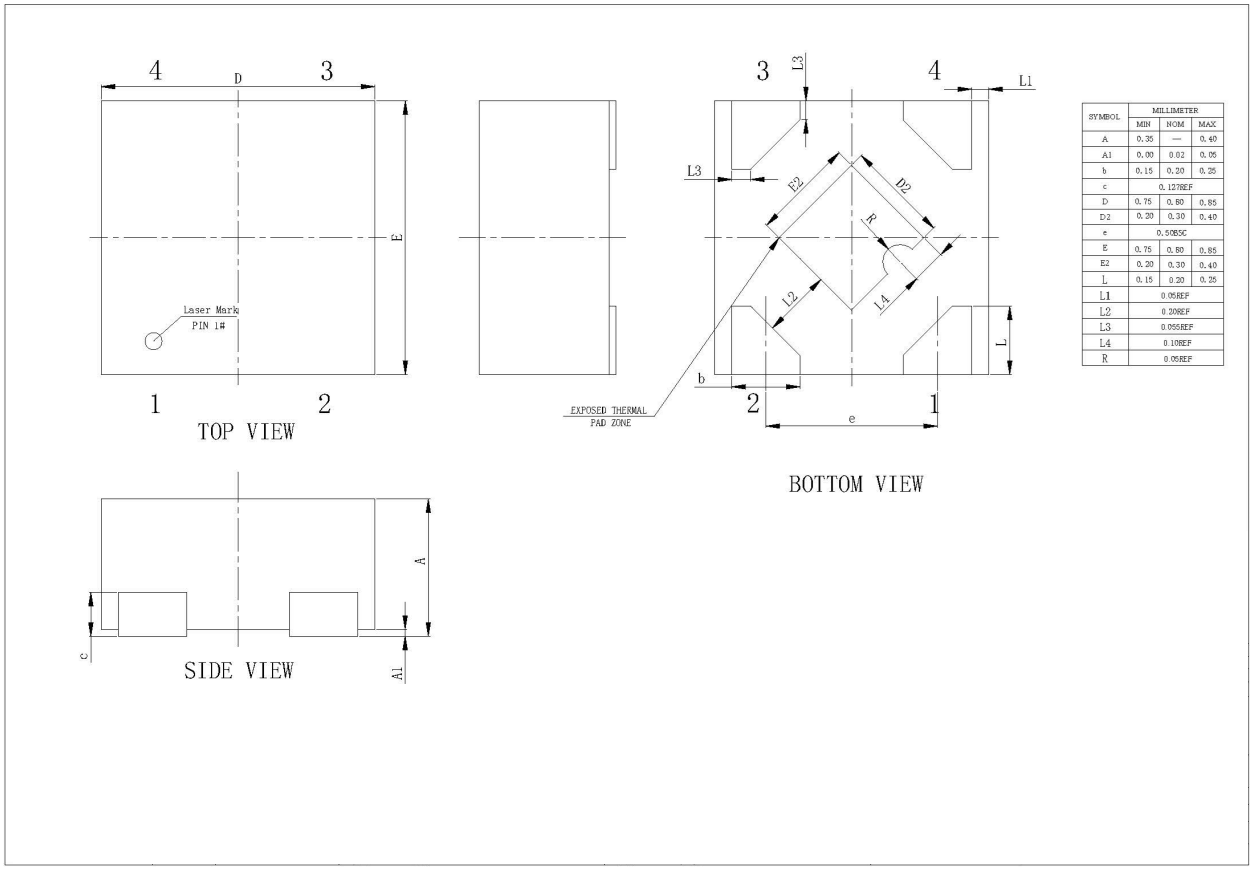
DFN1x1.45-6L



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		1 BSC	
	Y	E		1.45 BSC	
LEAD PITCH		e		0.5 BSC	
LEAD LENGTH		L	0.25	0.3	0.35
		L1		0.05 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.05	
LEAD OFFSET		bbb		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
4.FINISH: Cu/EP •Sn8~20s

DFN0.8x0.8-4L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.35	—	0.40
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	0.127REF		
D	0.75	0.80	0.85
D2	0.20	0.30	0.40
e	0.50BSC		
E	0.75	0.80	0.85
E2	0.20	0.30	0.40
L	0.15	0.20	0.25
L1	0.05REF		
L2	0.20REF		
L3	0.055REF		
L4	0.10REF		
R	0.05REF		

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision History

Table 11. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
EM74LVC1G38 Rev1.0	Oct 30, 2023	Product datasheet		