1. General Description

The EMP1105 is a low quiescent current,low-dropout regulator (LDO) that sources 500 mA current with good line and load transient. The EMP1105 is optimized for a wide variety of applications by supporting an input voltage range from 2.0 V to 5.5 V. EMP1105 is featured with low noise, high PSRR and low IQ that makes it is easily to be adopted in RF and high accuracy applications.

It is stable with small ceramic output capacitors allowing for a small overall solution size. All device versions have integrated thermal shutdown, current limit, and undervoltage lockout (UVLO). The device is available in a DFN1x1-4 and SOT23-5 package.

2. Features and Benefits

- 2.0V to 5.5V Input Voltage Range
- 1.2V to 3.6V Ouput Voltage Range
- 30µA Operating Quiescent Current
- Off State Current <100nA
- Max Output Current is Up to 500mA
- Low Drop Out Voltage: 240mV (Max) at 300mA (VOUT=3.3V)
- High PSRR: 70 dB at 1 kHz
- Stable With a 1µF Ceramic Output Capacitor
- EMP1105 available in DFN1X1-4 and SOT23-5 package

3. Applications

- Set-Top Boxes, TV, and Gaming Consoles
- Portable and Battery-Powered Equipment
- Desktop, Notebooks, and Ultrabooks
- Tablets and Remote Controls
- White Goods and Appliances
- Grid Infrastructure and Protection Relays
- Camera Modules and Image Sensors

4. Ordering information

Table 1 Ordering information

Type number	Output voltage	Topside marking	Package		
			Name	Description	Quantity
EMP110512DQN	1.2V	LACDYW	DFN1X1-4	DFN1X1 package, 4 pins 1mm x 1mm; 0.4 mm (Max) height	3000
EMP110512GV	1.2V	LACDYW	SOT23-5	SOT23 package, 5 pins 2.92mm x 2.8mm; 1.25 mm (Max) height	3000
EMP110515DQN	1.5V	LADDYW	DFN1X1-4	DFN1X1 package, 4 pins 1mm x 1mm; 0.4 mm (Max) height	3000
EMP110515GV	1.5V	LADDYW	SOT23-5	SOT23 package, 5 pins 2.92mm x 2.8mm; 1.25 mm (Max) height	3000
EMP110518DQN	1.8V	LAEDYW	DFN1X1-4	DFN1X1 package, 4 pins 1mm x 1mm; 0.4 mm (Max) height	3000
EMP110518GV	1.8V	LAEDYW	SOT23-5	SOT23 package, 5 pins 2.92mm x 2.8mm; 1.25 mm (Max) height	3000
EMP110525DQN	2.5V	LAFDYW	DFN1X1-4	DFN1X1 package, 4 pins 1mm x 1mm; 0.4 mm (Max) height	3000
EMP110525GV	2.5V	LAFDYW	SOT23-5	SOT23 package, 5 pins 2.92mm x 2.8mm; 1.25 mm (Max) height	3000
EMP110528DQN	2.8V	LAGDYW	DFN1X1-4	DFN1X1 package, 4 pins 1mm x 1mm; 0.4 mm (Max) height	3000
EMP110528GV	2.8V	LAGDYW	SOT23-5	SOT23 package, 5 pins 2.92mm x 2.8mm; 1.25 mm (Max) height	3000
EMP110530DQN	3.0V	LAHDYW	DFN1X1-4	DFN1X1 package, 4 pins 1mm x 1mm; 0.4 mm (Max) height	3000
EMP110530GV	3.0V	LAHDYW	SOT23-5	SOT23 package, 5 pins 2.92mm x 2.8mm; 1.25 mm (Max) height	3000
EMP110533DQN	3.3V	LAIDYW	DFN1X1-4	DFN1X1 package, 4 pins 1mm x 1mm; 0.4 mm (Max) height	3000
EMP110533GV	3.3V	LAIDYW	SOT23-5	SOT23 package, 5 pins 2.92mm x 2.8mm; 1.25 mm (Max) height	3000
EMP110536DQN	3.6V	LAJDYW	DFN1X1-4	DFN1X1 package, 4 pins 1mm x 1mm; 0.4 mm (Max) height	3000
EMP110536GV	3.6V	LAJDYW	SOT23-5	SOT23 package, 5 pins	3000

				2.92mm x 2.8mm; 1.25 mm (Max) height	
EMP1105A12GV	ADJ	LASDYW	SOT23-5	SOT23 package, 5 pins 2.92mm x 2.8mm; 1.25 mm (Max) height	3000
EMP1105A08GV	ADJ	LARDYW	SOT23-5	SOT23 package, 5 pins 2.92mm x 2.8mm; 1.25 mm (Max) height	3000

5. Function diagram

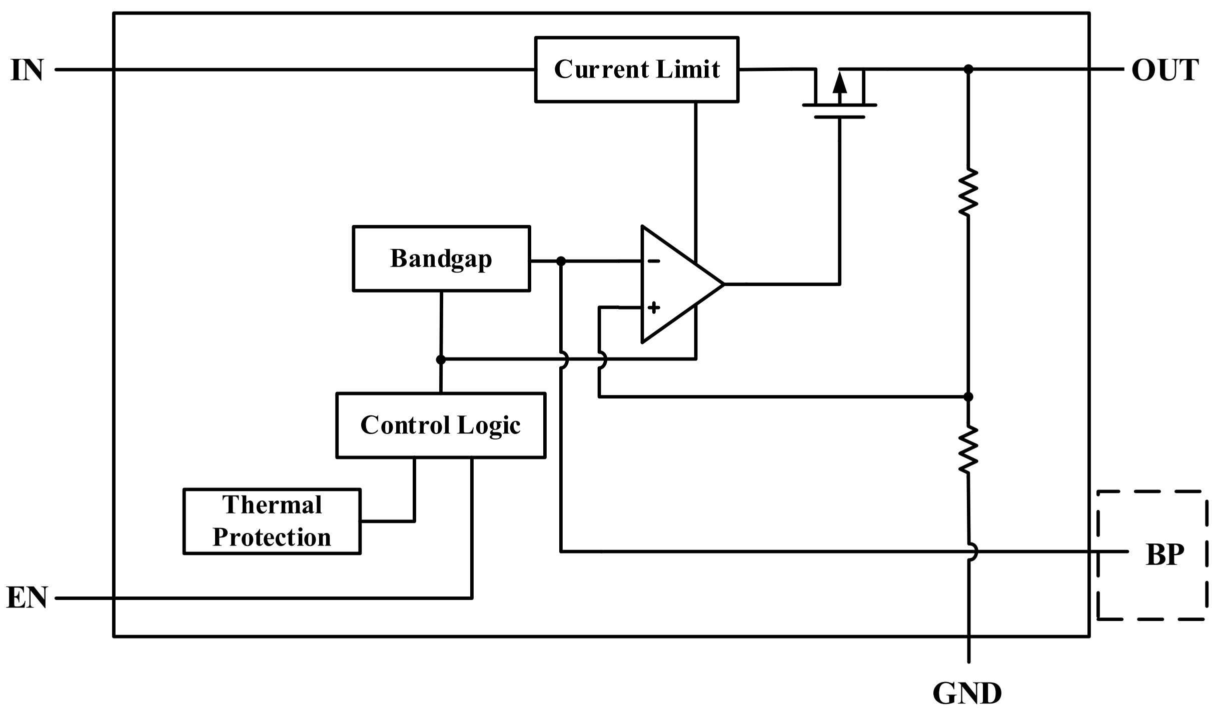


Fig 1. EMP1105XX function diagram

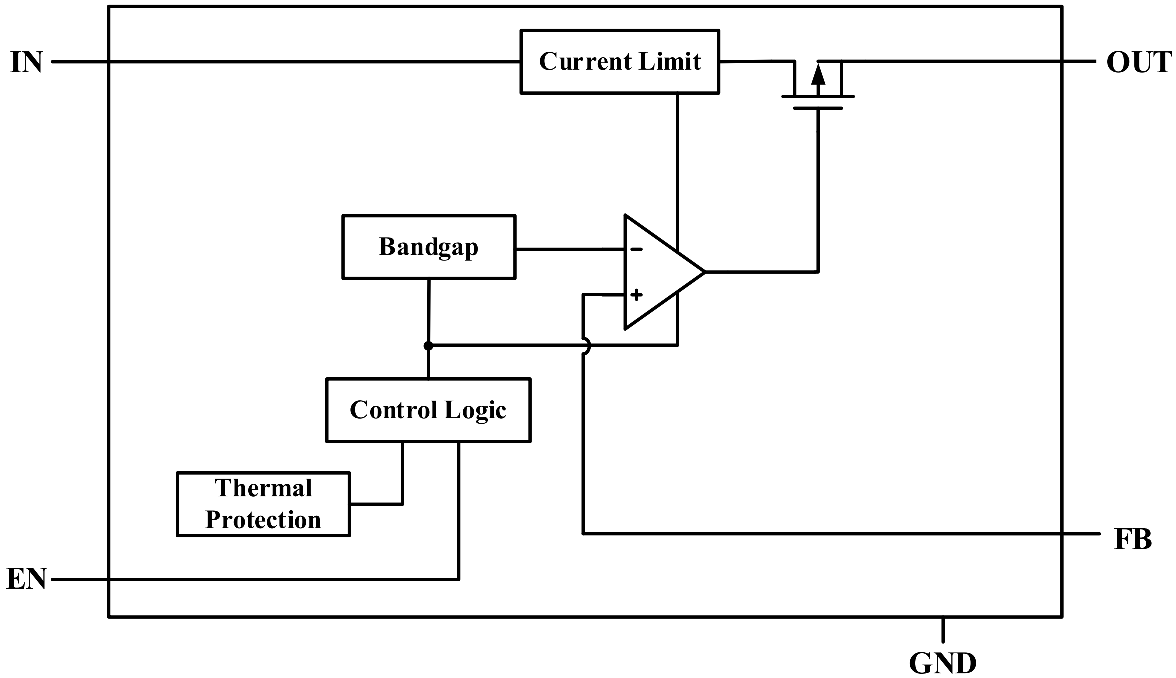


Fig 2. EMP1105AXX function diagram

6. Pinning information

6.1. Pin map

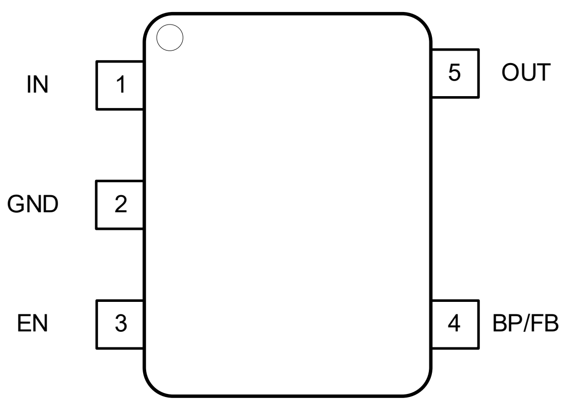


Fig 3. SOT23-5 top view pin map

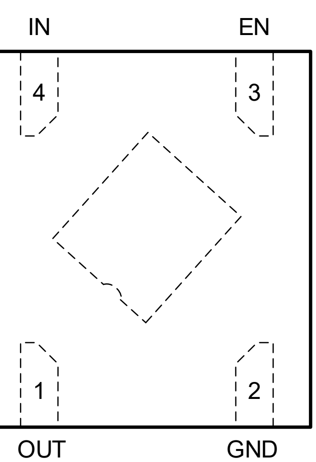


Fig 4. DFN1X1-4 top view pin map

6.2. Pin description

Table 2 Pin description

<table>
<tr><th>Pin Name</th><th>SOT23-5 Package</th><th>DFN1X1-4 Package</th><th>Type</th><th>Description</th></tr>
<tr><td>EN</td><td>3</td><td>3</td><td>Input</td><td>Device enable logic input. Logic high enables the device, logic low disables the device and turns it into shutdown.</td></tr>
<tr><td>GND</td><td>2</td><td>2</td><td>Power</td><td>Ground Pin</td></tr>
<tr><td>OUT</td><td>5</td><td>1</td><td>Power</td><td>Regulated output voltage pin. A capacitor with a value of 1 µF or larger is required from this pin to ground</td></tr>
<tr><td>IN</td><td>1</td><td>4</td><td>Power</td><td>Input pin. A capacitor with a value of 1 µF or larger is required from this pin to ground</td></tr>
<tr><td>BP</td><td rowspan="2">4</td><td>-</td><td>Output</td><td>Output bypass for the internal reference. Connect a low-ESR bypass ceramic capacitor of 0.01 µF from this pin to GND. Only for EMP1105XXGV.</td></tr>
<tr><td>FB</td><td>-</td><td>Input</td><td>Output voltage feedback pin connected to the error amplifier. Only for EMP1105AXXGV.</td></tr>
</table>

7. Functional description

The EMP1105 is a high PSRR and low noise low-dropout regulators (LDOs). This device consumes low quiescent current and delivers excellent line and load transient performance. EMP1105 supports wide input voltage range from 2V to 5.5 V. To minimize cost and solution size, the device is offered in fixed output voltages ranging from 1.2V to 3.6V to support different power requirement in applications. This regulator offers current limit, shutdown, and thermal protection.

7.1. EN Pin

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed VHI. Turn off the device by forcing the EN pin below VLO. If shutdown capability is not required, connect EN to IN.

7.2. Current Limit

EMP1105 family features an internal current limit. In normal operation, the the device limits output current to approximately 700mA. When current limiting engages, the output voltage scales back linearly until th e over current condition ends.

7.3. Thermal Shutdown

The device enters thermal shutdown once the junction temperature exceeds the thermal shutdown rising threshold, T_{JSD}. Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

8. Application Diagram

8.1. Input capacitor selection

The device requires a 1 µF or greater capacitor on the input pin. Some input supplies have a high impedance. Placing a capacitor on the input supply reduces the input impedance. The input capacitor counteracts reactive input sources and improves transient response and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors are used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are expected, or if the device is located several inches from the input power source.

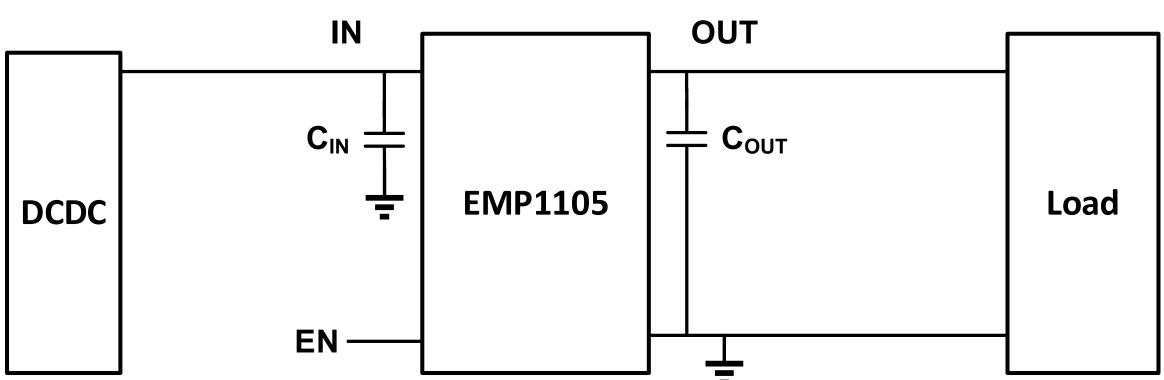


Fig 5. EMP1105XXDQN Application Diagram

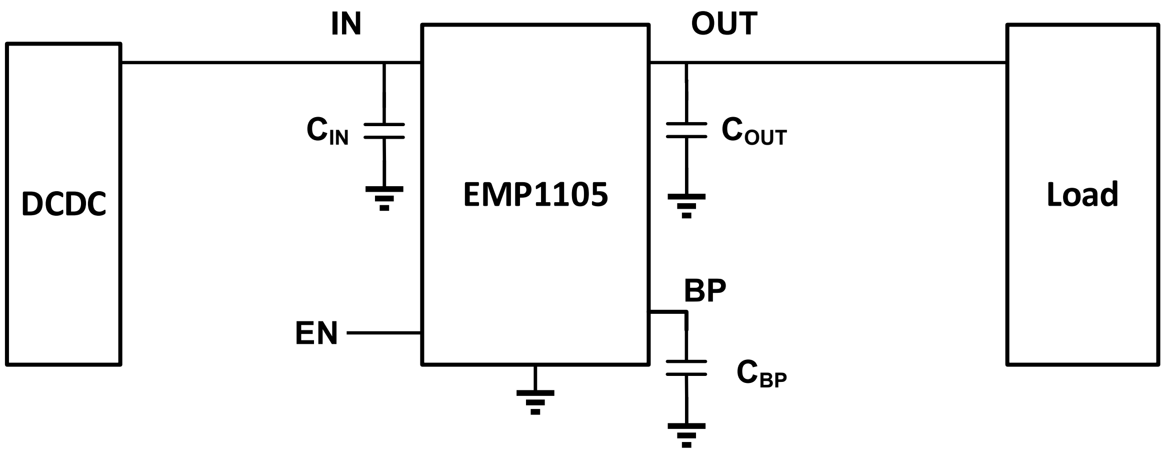


Fig 6. EMP1105XXGV Application Diagram

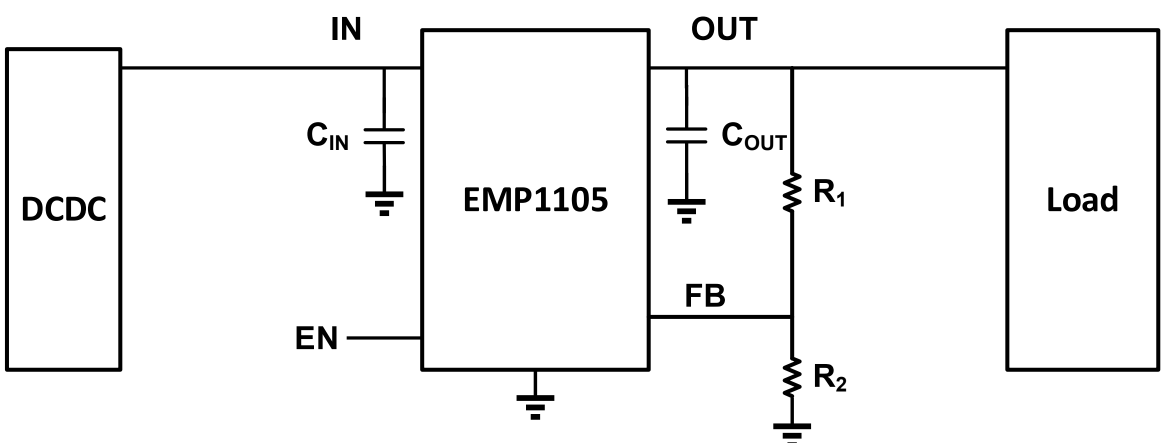


Fig 7. EMP1105AXXGV Application Diagram

8.2. Output capacitor selection

The EMP1105 requires an output capacitance of 0.47 µF or larger for stability. When selecting a capacitor for a specific application, consider the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. As a general rule, ceramic capacitors must be derated by 50%.

8.3. Setting the Output Voltage

For EMP1105AXXGV an external resistor divider is used to set output voltage according to Equation 1. When sizing R2, in order to achieve low current consumption and acceptable noise sensitivity, use a maximum of 160kΩ for EMP1105A08GV (V_{FB}=0.8V) and 240kΩ for EMP1105A12GV (V_{FB}=1.2V) .

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \tag{1}$$

8.4. Dropout voltage

The EMP1105 uses a PMOS pass transistor to achieve low dropout. When (VIN – VOUT) is less than the dropout voltage (VDO), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the RDSON of the PMOS. VDO scales linearly with the output current because the PMOS device functions like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (VIN – VOUT) approaches dropout operation.

8.5. Power dissipation

The power supply reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free of other heat-generating devices as possible that cause added thermal stresses. As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use the following equation to estimat PD:

$$PD = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{2}$$

Power dissipation must be minimized to achieve greater efficiency. This minimizing process is achieved by selecting the correct system voltage rails. Proper selection helps obtain the minimum input-to-output voltage differential. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

9. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 3 Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter	Conditions	Min	Max	Unit
V_I[1]	Input voltage	VIN	-0.3	+7.0	V
		EN	-0.3	VIN	V
V_O[1]	Output voltage	VOUT	-0.3	VIN	V
T_{stg}	Storage temperature		-65	150	°C
T_J	Junction temperature			150	°C
ESD	HBM	ANSI/ESDA/JEDEC JS-001 Class 2	4		kV
	CDM	ANSI/ESDA/JEDEC JS-002	500		V

[1] All voltage values, except differential voltages, are with respect to network ground terminal.

10. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 4 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	Input voltage		2		5.5	V
T_{amb}	Ambient Operating temperature		-40		+85	°C

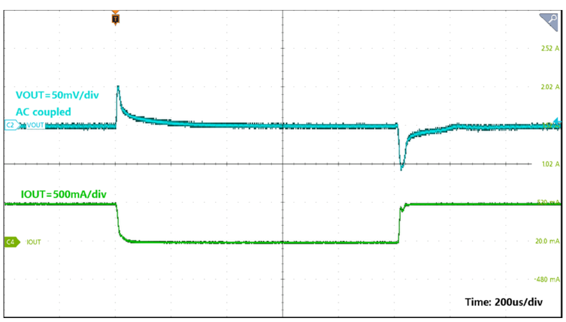
11. Electrical Characteristics

T_{amb} = -40°C to 85°C unless otherwise indicated. V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF, unless otherwise noted. All typical values at T_{amp} = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Input Voltage			2.0		5.5	V
V_{OUT}	Output Voltage			1.2		3.6	V
Output accuracy	Output voltage accuracy	I_{OUT}=0.1mA		-2		2	%
V_{FB}	Feedback regulation voltage	I_{OUT}=0.1mA, EMP1105A08GV		0.783	0.8	0.815	V
		I_{OUT}=0.1mA, EMP1105A12GV		1.179	1.203	1.227	V
V_{LNR}	Line regulation	V_{IN} =V_{OUT}+0.5V ~5.5V I_{OUT}=1mA			0.1	0.2	%
V_{LDR}	Load regulation	I_{OUT} =0.1mA ~500mA, C_{OUT}=1µF			25	50	mV
		I_{OUT} =0.1mA ~500mA, C_{OUT}=1µF, EMP1105AXXGV			0.5	10	mV
I_Q	Static current				30	40	uA
I_{SHDN}	Shutdown current	V_{EN}=0V			0.01	1	µA
$I_{OUT(MAX)}$	Maximum output current			500			mA
V_{DROP}	Dropout voltage	I_{OUT}=500mA, V_{OUT}=1.2V			900		mV
		I_{OUT}=500mA, V_{OUT}=1.5V			630		mV
		I_{OUT}=500mA, V_{OUT}=3.3V			450	600	mV
e_N	V_{OUT} noise	f=10Hz ~100KHz C_{OUT}=10uF I_{OUT}=30mA			90		µ V_{RMS}
PSRR	Power supply ripple rejection	C_{BP}=0uF I_{LOAD}=30mA C_{OUT}=1uF V_{IN}=V_{OUT}+1V ΔV_{RIPPLE}=0.2V_{PP}	f=217Hz		72		dB
			f=1kHz		70		
		C_{BP}=10nF I_{LOAD}=30mA C_{OUT}=1uF V_{IN}=V_{OUT}+1V ΔV_{RIPPLE}=0.2V_{PP}	f=217Hz		74		dB
			f=1kHz		70		
V_{IH}		V_{IN}=2V		1.2			V

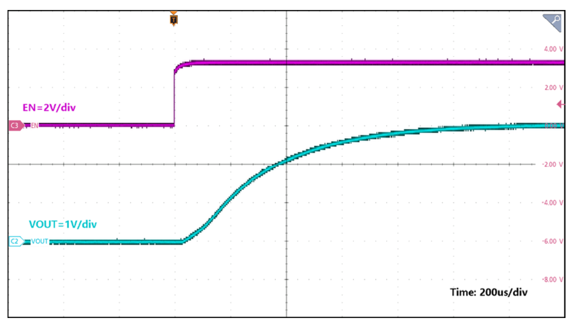
	EN pin high voltage(enabled)	V_{IN}=5.5V	2			V
V_{IL}	EN pin low voltage(disabled)	V_{IN}=2V			0.4	V
		V_{IN}=5.5V			0.6	V
I_{EN}	Enable pin current	EN=5.5V		0.01	1	µA
Thermal Protection						
T_{THMP}	Over temperature shutdown threshold			150		°C
T_{THMP_HYS}	Over temperature shutdown hysteresis			15		°C
Timing specifications						
t_{STR}	Startup time	C_{OUT}=1uF, no load		500		us

11.1. Testing waveforms



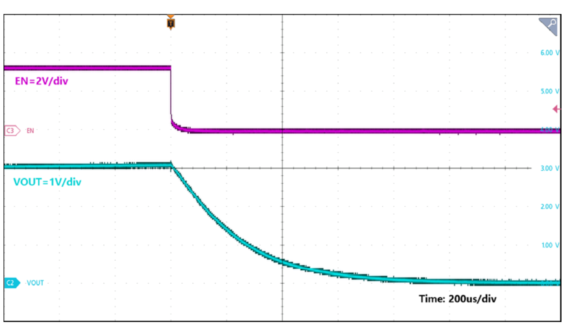
V_{IN}=3.8V, V_{OUT}=3.3V, IOUT slew rate=1A/us

Fig 8. 3.3V, 0mA to 500mA Load Transient



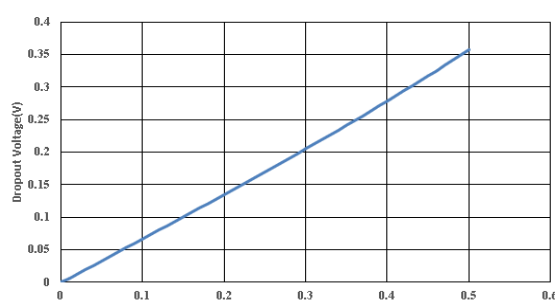
V_{IN}=3.8V, V_{OUT}=3.3V, Ta=25℃

Fig 9. Startup



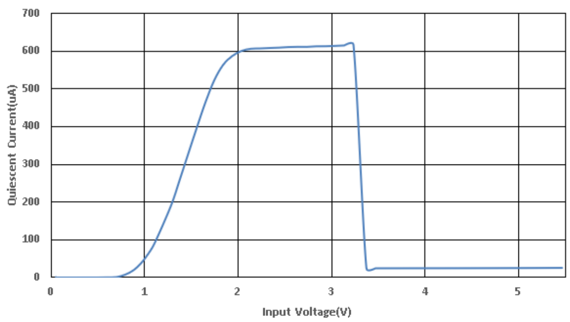
V_{IN}=3.8V, V_{OUT}=3.3V, Ta=25℃

Fig 10. Shutdown



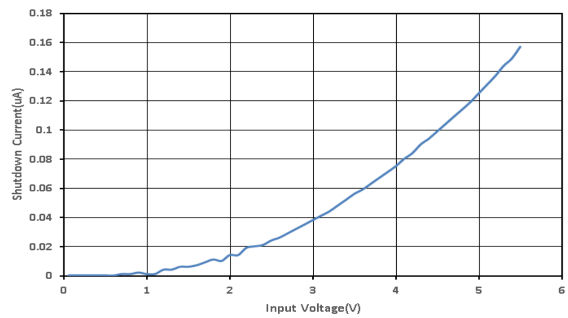
Vout=3.3V, Ta=25℃

Fig 11. Dropout vs I_{OUT}



V_{OUT}=3.3V, I_{OUT}=0mA, Ta=25℃

Fig 12. I_Q vs V_{IN}



V_{OUT}=3.3V, I_{OUT}=0mA, Ta=25℃

Fig 13. I_{SHDN} vs V_{IN}

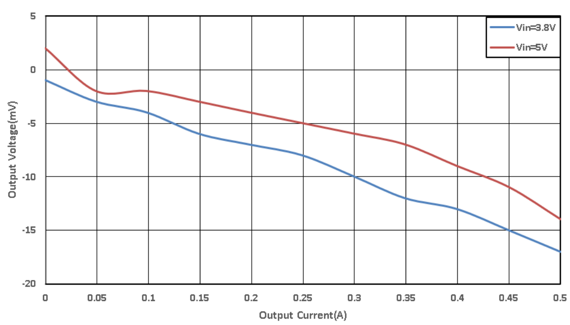
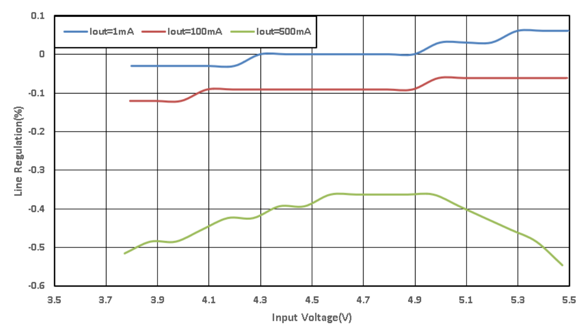


Fig 14. Load Regulation vs I_{OUT}

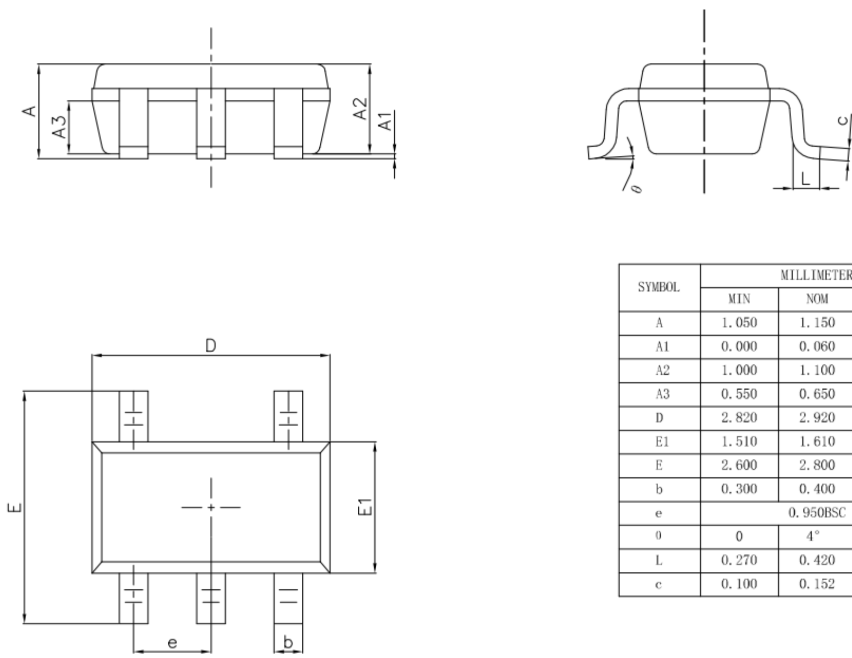


V_{OUT}=3.3V, Ta=25℃

Fig 15. Line Regulation vs V_{IN}

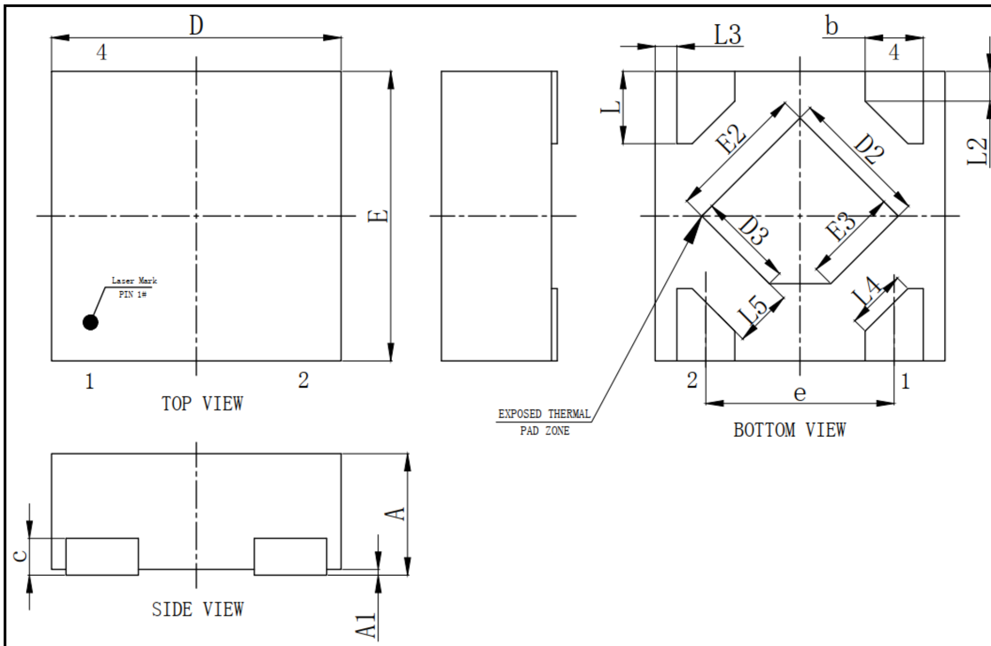
12. Package outline

SOT23-5



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.050	1.150	1.250
A1	0.000	0.060	0.150
A2	1.000	1.100	1.200
A3	0.550	0.650	0.750
D	2.820	2.920	3.020
E1	1.510	1.610	1.710
E	2.600	2.800	3.000
b	0.300	0.400	0.500
e	0.950BSC		
θ	0	4°	8°
L	0.270	0.420	0.570
c	0.100	0.152	0.200

DFN1X1-4



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.35	-	0.40
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	0.127REF		
D	0.95	1.00	1.05
D2	0.38	0.48	0.58
D3	0.23	0.33	0.43
e	0.65BSC		
E	0.95	1.00	1.05
E2	0.38	0.48	0.58
E3	0.23	0.33	0.43
L	0.20	0.25	0.30
L2	0.103REF		
L3	0.075REF		
L4	0.208REF		
L5	0.200REF		

13. Abbreviations

Table 5 Abbreviations

Acronym	Description
CDM	Charged Device Model
HBM	Human Body Model

14. Revision history

Table 6 Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
EMP1105 Rev1.0	Dec 08, 2022	Product datasheet		