EMS4422

2:1 Mux/DeMux High Bandwidth HDMITM 2.1 Compliant Signal Switch

Product datasheet, Rev. 1.0 Feb 13, 2025

1.General Description

The EMS4422 series of switch circuits are targeted for high-resolution video network that are based on DVI/HDMI™ standard, and TMDS signal process. The EMS4422 is an 8 to 4 Channel Mux/DeMux Switch. The device multiplexes differential signals to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high speed signals at the outputs. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation.

The high bandwidth provides the resolution required by the next generation HDTV and PC graphics. Three differential channels are used for data (video signals for DVI or audio/video signals for HDMI), and one differential channel is used for Clock for decoding the TMDS signals at the outputs.

Because of its passive bidirectional feature, this switch can be used either at the video drivers side or at the receiver side. For PC graphics applications, the device sits at the drivers side to switch between multiple display units such as LCD monitor, projector, TV, etc. For consumer video applications, the device sits at the receiver end to switch between the source components such as DVD, D-VHS, STB, etc.

The wide voltage range allow DC-coupled multi-standard operation. Eliminating AC coupling capacitors saves board space and improves signal integrity for dense PCB design. The high speed channels can also pass 0V-3.3V CMOS signals up to 1MHz. In addition to four high speed lanes, EMS4422 also switches the DDC and HPD signals.

2.Features and Benefits

- 4-Differertial Channel 2:1 Mux/DeMux
- HDMIT 2.1 compatible
- High Bandwidth: 5.7GHz @-3dB BW
- Supports both AC coupled and DC coupled signals
- Isolation: -40dB @ 2.0 Gbps
- Crosstalk: -31dB @ 2.0 Gbps
- ESD Tolerance: 2kV HBM
- Low bit-to-bit skew, Bidirectional
- Supports DDC with HPD channel mux/demux @ HDMI
- Supports 720 Mbps high-speed DP AUX @ DP

3.Applications

- Routing of HDMI 2.1 video signals with low signal attenuation between source and sink for 4K 2K ultra high definition video display and broadcast video equipment.
- Routing of DisplayPort video signals with low signal attenuation between source and sink for PC and monitor.

4.Ordering Information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Quantity
EMS4422RSE	A422	QFN5×5-20L	QFN package, 20 pins 5 mm × 5 mm; 0.8 mm (Max) height	3000

5.Function Diagram

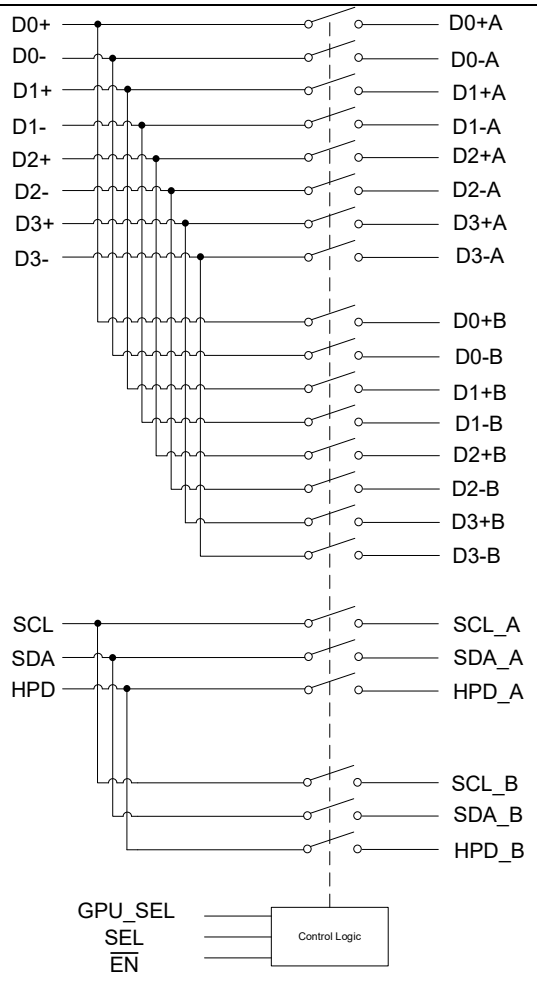


Fig 1. Block Diagram

6.Pinning Information

6.1. Pin map

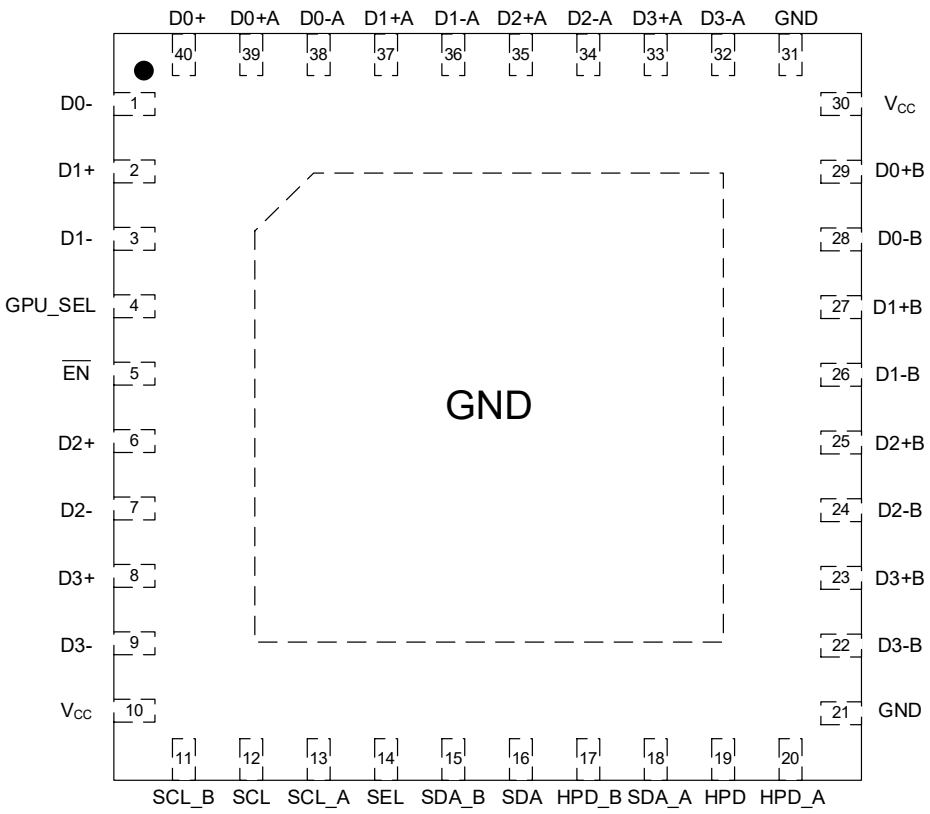


Fig 2. Top view pin configuration
QFN 1.8x2.6 -16L

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
D0+	40	Positive differential signal 0 for COM port
D0-	1	Negative differential signal 0 for COM port
D1+	2	Positive differential signal 1 for COM port
D1-	3	Negative differential signal 1 for COM port
GPU_SEL	4	GPU Switch logic control
_EN	5	Chip Enable, Active low
D2+	6	Positive differential signal 2 for COM port
D2-	7	Negative differential signal 2 for COM port
D3+	8	Positive differential signal 3 for COM port
D3-	9	Negative differential signal 3 for COM port
VCC	10,30	Supply Voltage
SCL_B	11	DDC clock for port B
SCL	12	DDC clock for COM port
SCL_A	13	DDC clock for port A
SEL	14	Switch logic control for DDC/AUX and HPD
SDA_B	15	DDC data for port B
SDA	16	DDC data for COM port
HPD_B	17	Hot plug detect for B port
SDA_A	18	DDC data for port A
HPD	19	Hot plug detect for COM port
HPD_A	20	Hot plug detect for port A
GND	21,31	Ground
D3-B	22	Negative differential signal 3 for port B
D3+B	23	Positive differential signal 3 for port B
D2-B	24	Negative differential signal 2 for port B
D2+B	25	Positive differential signal 2 for port B
D1-B	26	Negative differential signal 1 for port B
D1+B	27	Positive differential signal 1 for port B

Symbol	Pin	Description
D0-B	28	Negative differential signal 0 for port B
D0+B	29	Positive differential signal 0 for port B
D3-A	32	Negative differential signal 3 for port A
D3+A	33	Positive differential signal 3 for port A
D2-A	34	Negative differential signal 2 for port A
D2+A	35	Positive differential signal 2 for port A
D1-A	36	Negative differential signal 1 for port A
D1+A	37	Positive differential signal 1 for port A
D0-A	38	Negative differential signal 0 for port A
D0+A	39	Positive differential signal 0 for port A

7.Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input $\overline{EN}$	Input GPU_SEL	Function (D0 to D3)
H	X	Switch disabled. All channels are Hi-Z.
L	L	All A channels are enabled. All B channels are Hi-Z.
L	H	All B channels are enabled. All A channels are Hi-Z.

Input $\overline{EN}$	Input SEL	Function (SCL, SDA, HPD)
H	X	Switch disabled. All channels are Hi-Z.
L	L	All A channels are enabled. All B channels are Hi-Z.
L	H	All B channels are enabled. All A channels are Hi-Z.

8.Absolute Maximum Ratings

Absolute Maximum Ratings may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		-0.5	5.5	V
V_{SW-HS}	High Speed Switch Voltage Range (Data Channels)		-0.5	3.8	
V_{SW-LS}	Low Speed Switch Voltage Range (Sideband Channels)		-0.5	5.5	
V_{IN}	Digital Input Voltage Range		-0.3	V_{CC}	V
I_C	On-State Switch Current			±120	mA
P_D	power dissipation			500	mW
T_{stg}	storage temperature		-65	150	°C
T_J	junction temperature under bias			125	°C

9.Recommended Operating Conditions

Table 5. Recommend operating ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		1.5		5.0	V
V_{SW-HS}	High Speed Switch I/O Voltage		0		3.3	V
V_{SW-LS}	Low Speed Switch I/O Voltage		0		V_{CC}+0.3	
V_{IN}	Control Input Voltage		0		5.0	V
T_A	Operating Temperature		-40		85	°C

10. Electrical Characteristics

Table 6. Static characteristics

T_A = 25℃, V_{CC} = 3.3V, unless otherwise specified

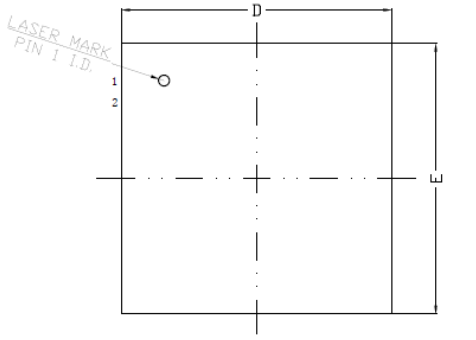
Symbol	Parameter		Conditions	Min	Typ	Max	Unit
PORT A							
R_{ON}	on-resistance	D0 to D3	V_{CC} = 3V, 1.5V≤$V_{I/O}$≤V_{CC}, $I_{I/O}$=-40mA		6.5	9.5	Ω
		SCL,SDA,HPD			6	9.5	Ω
$R_{ON(flat)}$	ON-state resistance flatness	All I/O	V_{CC}=3V, $V_{I/O}$ =1.5V and V_{CC},$I_{I/O}$=-40mA		1.5		Ω
ΔR_{ON}	On-state resistance match between high-speed channels	D0 to D3	V_{CC}=3V, 1.5V≤$V_{I/O}$≤V_{CC}, $I_{I/O}$=-40mA		0.4	1	Ω
I_{OFF}	Leakage under power off	All outputs	V_{CC}=0V, $V_{I/O}$ =0V to 3.6V , V_{IN}=0V to 5.5V			±10	uA
PORT B							
R_{ON}	on-resistance	D0 to D3	V_{CC} = 3V, 1.5V≤$V_{I/O}$≤V_{CC}, $I_{I/O}$=-40mA		8.2	10.5	Ω
		SCL,SDA,HPD			6	9.5	Ω
$R_{ON(flat)}$	ON-state resistance flatness	All I/O	V_{CC}=3V, $V_{I/O}$ =1.5V and V_{CC},$I_{I/O}$=-40mA		1.5		Ω
ΔR_{ON}	On-state resistance match between high-speed channels	D0 to D3	V_{CC}=3V, 1.5V≤$V_{I/O}$≤V_{CC}, $I_{I/O}$=-40mA		0.4	1	Ω
I_{OFF}	Leakage under power off	All outputs	V_{CC}=0V, $V_{I/O}$ =0V to 3.6V , V_{IN}=0V to 5.5V			±10	uA

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
DIGITAL INPUTS							
V_{IH}	High-level control input voltage	GPU_SEL, SEL, $\overline{EN}$		1.4			V
V_{IL}	LOW-level control input voltage					0.5	V
V_{IH}	Digital input high leakage current		V_{CC}=3.6V, V_{IN}=V_{CC}			±10	uA
V_{IL}	Digital input low leakage current		V_{CC}=3.6V, V_{IN}=GND			±10	uA
SUPPLY							
I_{CC}	V_{CC} supply current		V_{CC}=3.6V, $I_{I/O}$ =0,Normal operation mode, $\overline{EN}$=L		100		uA
I_{CC-PD}	V_{CC} supply current in power-down mode		V_{CC}=3.6V, $I_{I/O}$ =0, $\overline{EN}$=H		2		uA
AC Characteristics							
t_{pd}	Propagation delay (input pin to output pin) on all channels				80		ps
t_{b-b}	Bit-to-bit skew within the same differential pair of Dx± channels				5	7	ps
t_{ch-ch}	Channel-to-channel skew of Dx+ channels					35	ps
t_{sw}	Time it takes to switch from port A to port B					0.1	us
	Time it takes to switch from port B to port A					0.1	us
$t_{startup}$	VCC valid to channel enable					10	us
t_{wakeup}	Enabling output by changing OE from low to High					10	us

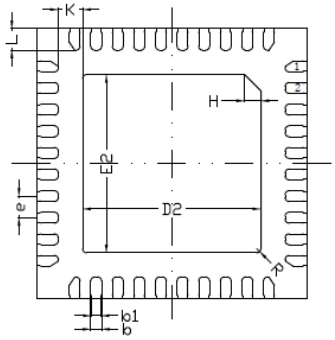
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
X_{TALK}	Crosstalk on High Speed Channels	f = 3.0GHz		-25	-22	dB
		f = 2.7GHz		-28	-25	
		f = 1.7GHz		-31	-28	
		f = 1.35GHz		-32	-28	
O_{IRR}	OFF Isolation on High Speed Channels	f = 3.0GHz		-22	-20	
		f = 2.7GHz		-22	-20	
		f = 1.7GHz		-29	-26	
		f = 1.35GHz		-30	-27	
I_{LOSS}	Different Insertion Loss on High Speed Channels	f = 3.0GHz	-2.0	-1.7		dB
		f = 5.4GHz	-2.0	-1.7		
R_{LOSS}	Different Return Loss on High Speed Channels	f = 3.0GHz(6.0Gbps)		-16.0	-14	dB
		f = 2.7GHz(5.4Gbps)		-14.0	-12.5	
BW	Bandwidth -3dB			5.7		GHz

11. Package Outline

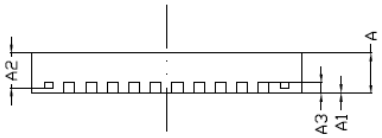
QFN 5x5 -40L



TOP VIEW



BOTTOM VIEW



SIDE

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	--	0.02	0.05
A2	0.60	0.65	0.70
A3	0.20REF		
b	0.15	0.20	0.25
b1	0.18REF		
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.20	3.30	3.40
E2	3.20	3.30	3.40
e	0.40BSC		
H	0.25	0.30	0.35
K	0.45REF		
L	0.35	0.40	0.45
R	0.075REF		

12. Revision History

Table 7. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
EMS4422 Rev. 1.0	Feb 13, 2025	Product datasheet		