

1. General Description

The EM74HC597; EM74HCT597 is an 8-bit shift register with input flip-flops. It consists of an 8-bit storage register feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive edge-triggered clocks. The shift register also has direct load (from storage) and clear inputs. Inputs include clamp diodes, this enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and Benefits

- Wide supply voltage range from 2.8 V to 6.0 V
- High noise immunity
- CMOS low power dissipation
- 8-bit parallel storage register inputs
- Shift register has direct overriding load and clear
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standard:
 - JESD8C(2.8 V to 3.6 V)
 - JESD7A(2.8 V to 6.0 V)
- Input levels:
 - For EM74HC597: CMOS level
 - For EM74HCT597: TTL level
- ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 3500 V
 - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

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3. Ordering Information

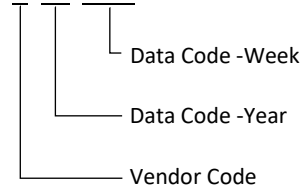
Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Quantity
EM74HC597D	HC597 YYYWW	SOP-16L	plastic small outline package; 16 leads; body width 3.9 mm	3000
EM74HCT597D	HCT597 YYYWW			
EM74HC597PW	HC597 YYYWW	TSSOP-16L	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	3000
EM74HCT597PW	HCT597 YYYWW			

MARKING INFORMATION

NOTE: YYYWW = Vendor Code and Data Code.

X YY WW



4.Function Diagram

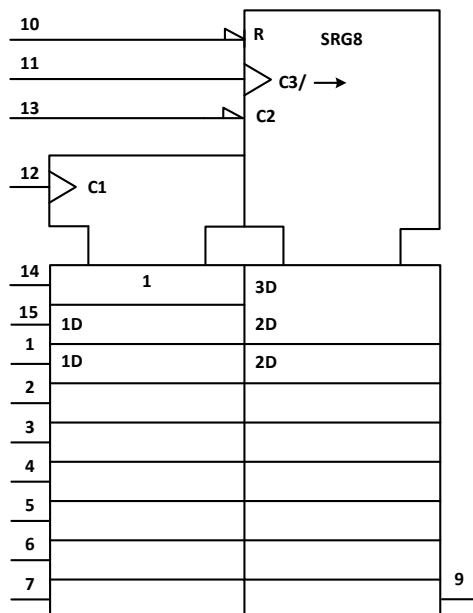
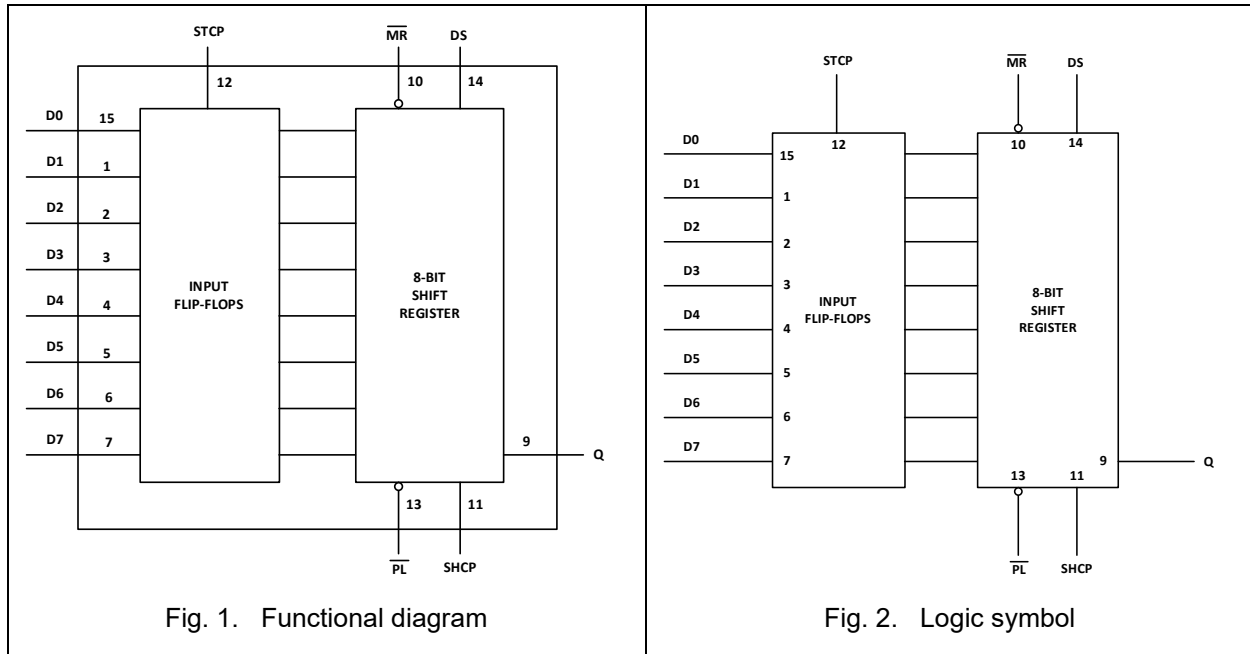
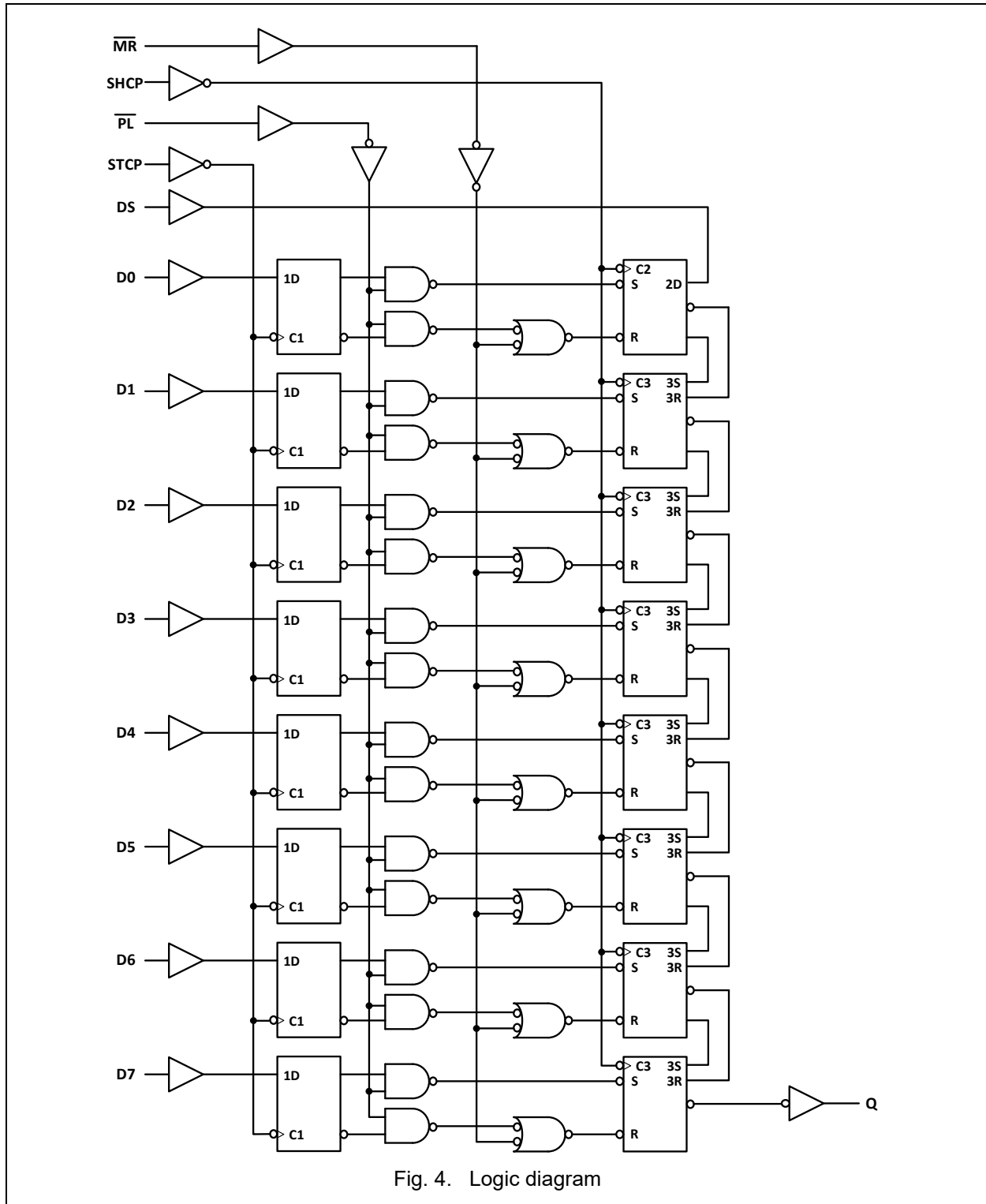


Fig. 3. IEC Logic symbol

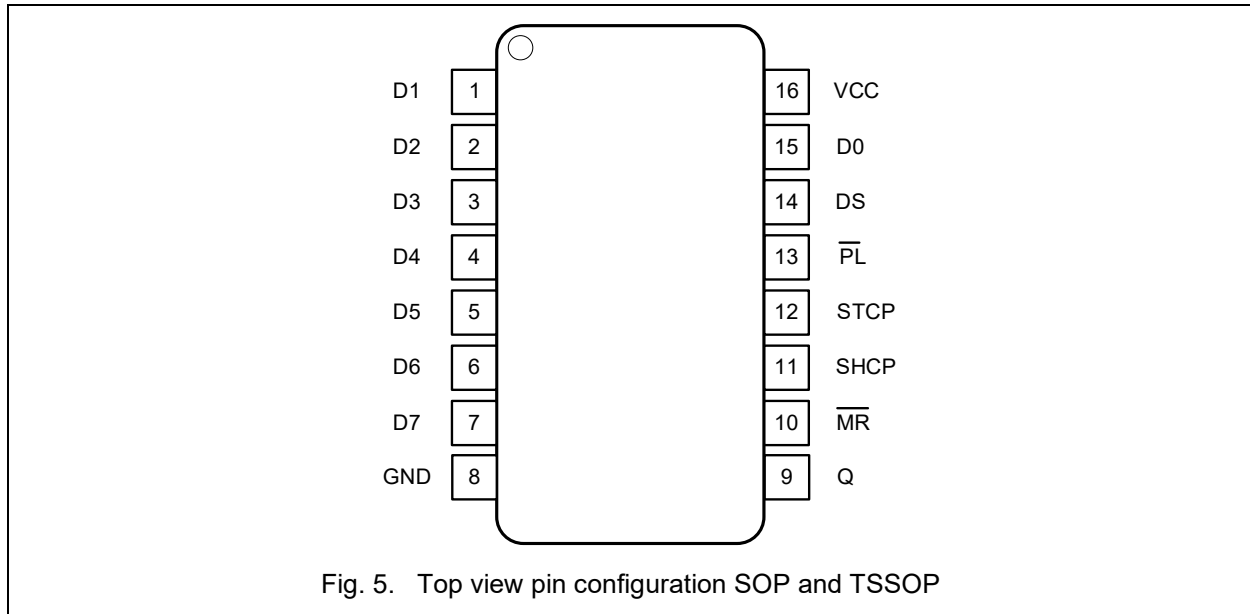
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5. Pinning Information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
GND	8	ground(0V)
Q	9	serial data output
$\overline{\text{MR}}$	10	asynchronous master reset input (active LOW)
SHCP	11	shift register clock input (LOW-to-HIGH, edge-triggered)
STCP	12	storage register clock input (LOW-to-HIGH, edge-triggered)
$\overline{\text{PL}}$	13	parallel load input (active LOW)
DS	14	serial data input
D0,D1,D2,D3,D4,D5,D6,D7	15,1,2,3,4,5,6,7	parallel data inputs
V _{CC}	16	supply voltage

6. Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition.

Inputs				Function
STCP	SHCP	$\overline{\text{PL}}$	$\overline{\text{MR}}$	
↑	X	X	X	data loaded to input latches
↑	X	L	H	data loaded from inputs to shift register
no clock edge	X	L	H	data transferred from input flip-flops to shift register
X	X	L	L	invalid logic, state of shift register is indeterminate when signals removed
X	X	H	L	shift register cleared
X	↑	H	H	shift register clocked $Q_n = Q_{n-1}$, $Q_0 = \text{DS}$

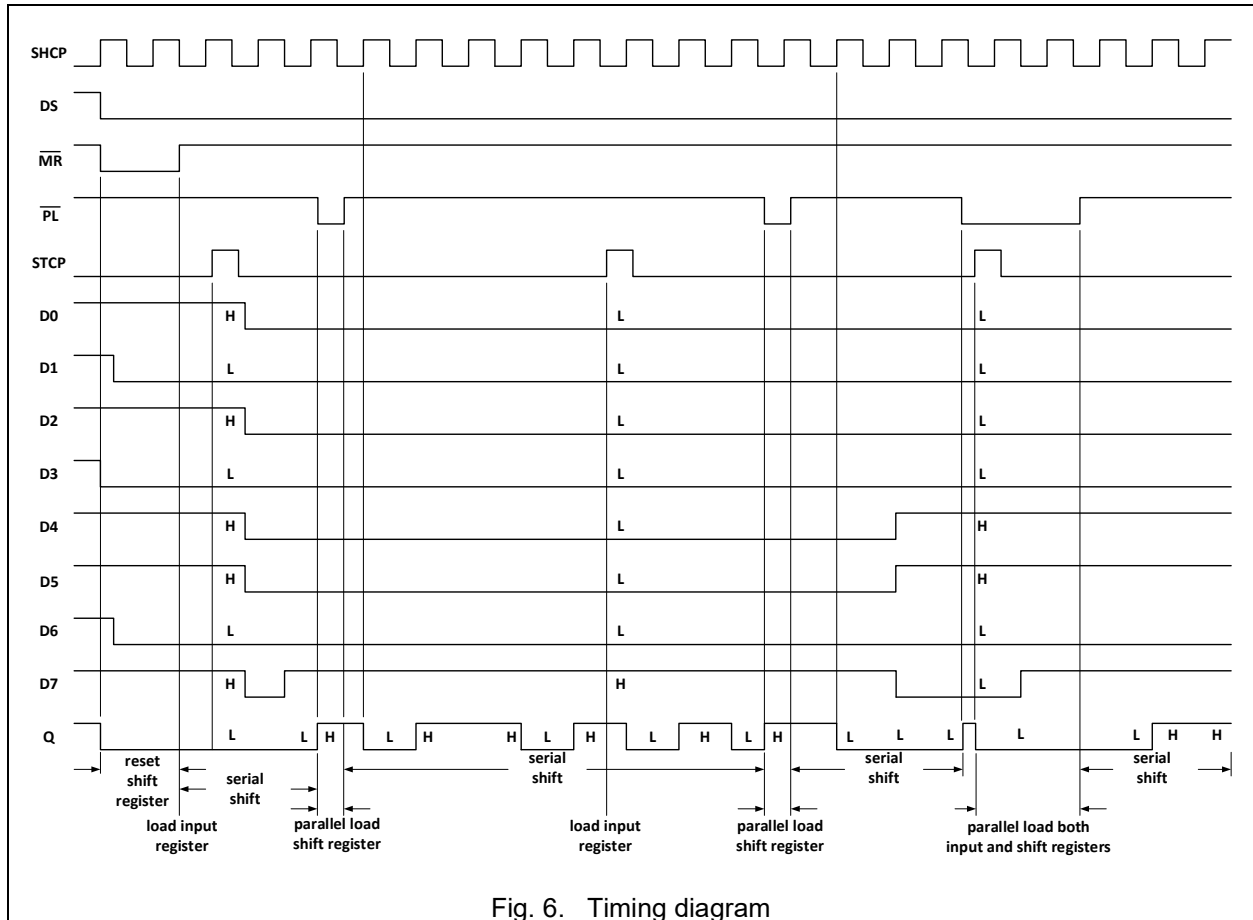


Fig. 6. Timing diagram

7. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	7.0	V
I_{IK}	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$ [1]		± 20	mA
I_{OK}	output clamping current	$V_O < -0.5 \text{ V}$ or $V_O > V_{CC} + 0.5 \text{ V}$ [1]		± 20	mA
I_O	output current	$-0.5 \text{ V} < V_O < V_{CC} + 0.5 \text{ V}$		± 25	mA
I_{CC}	supply current			50	mA
I_{GND}	ground current		-50		mA
P_{tot}	total power dissipation	$T_{amb} = -40 \text{ }^\circ\text{C}$ to $+125 \text{ }^\circ\text{C}$		500	mW
T_{stg}	storage temperature		-65	150	$^\circ\text{C}$

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	EM74HC597			EM74HCT597			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.8	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0		V_{CC}	0		V_{CC}	V
V_O	output voltage		0		V_{CC}	0		V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	$^\circ\text{C}$
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.0 \text{ V}$			371				ns/V
		$V_{CC} = 4.5 \text{ V}$		1.67	139		1.67	139	ns/V
		$V_{CC} = 6.0 \text{ V}$			83				ns/V

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9.Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
EM74HC597								
V _{IH}	HIGH-level input voltage	V _{CC} = 3.0 V	2.0	1.8		2.0		V
		V _{CC} = 4.5 V	3.15	2.4		3.15		V
		V _{CC} = 6.0 V	4.2	3.5		4.2		V
V _{IL}	LOW-level input voltage	V _{CC} = 3.0 V		1.3	0.6		0.6	V
		V _{CC} = 4.5 V		2.1	1.35		1.35	V
		V _{CC} = 6.0 V		2.8	1.8		1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -20μA; V _{CC} = 3.0 V	2.9	3.0		2.9		V
		I _O = -20μA; V _{CC} = 4.5 V	4.4	4.5		4.4		V
		I _O = -20μA; V _{CC} = 6.0 V	5.9	6.0		5.9		V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.84	4.4		3.7		V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.34	5.9		5.2		V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 20μA; V _{CC} = 3.0 V		0	0.1		0.1	V
		I _O = 20μA; V _{CC} = 4.5 V		0	0.1		0.1	V
		I _O = 20μA; V _{CC} = 6.0 V		0	0.1		0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V		0.04	0.33		0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V		0.05	0.33		0.4	V
I _I	input leakage current	V _I = V _{CC} or GND ; V _{CC} = 6.0 V		0.1	±1		±1	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0A ; V _{CC} = 6.0 V		11	20		40	μA
C _I	input capacitance	Pin $\overline{\text{PL}}$, $\overline{\text{MR}}$		4.5				pF
		Pin DS, STCP,SHCP		8.0				pF
		Pin D0 to D7		9.5				pF

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Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
EM74HCT597								
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.7		2.0		V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V		1.4	0.8		0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V						
		I _O = -20μA	4.4	4.5		4.4		V
		I _O = -4.0 mA	3.84	4.4		3.7		V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V						
		I _O = 20μA		0	0.1		0.1	V
		I _O = 4.0 mA		0.04	0.33		0.4	V
I _I	input leakage current	V _I = V _{CC} or GND ; V _{CC} = 5.5 V		0.1	±1		±1	μA
I _{CC}	supply current	V _I = V _{CC} or GND ; I _O = 0A ; V _{CC} = 5.5 V		11	20		40	μA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A			450		490	μA
C _i	input capacitance	Pin $\overline{PL}, \overline{MR}$		4.5				pF
		Pin DS, STCP, SHCP		8.0				pF
		Pin D0 to D7		9.5				pF

[1] All typical values are measured at $T_{amb} = 25^\circ\text{C}$.

10. Dynamic Characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 13.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
EM74HC597								
t _{pd}	propagation delay	SHCP to Q; see Fig. 7 [2]						
		V _{CC} = 3.0 V			27		30	ns
		V _{CC} = 4.5 V			17		20	ns
		V _{CC} = 6.0 V			13		15	ns
		$\overline{\text{MR}}$ to Q; see Fig. 8 [2]						
		V _{CC} = 3.0 V			27		30	ns
		V _{CC} = 4.5 V			17		20	ns
		V _{CC} = 6.0 V			13		15	ns
		STCP to Q;see Fig. 7 [2]						
		V _{CC} = 3.0 V			27		30	ns
		V _{CC} = 4.5 V			17		20	ns
		V _{CC} = 6.0 V			13		15	ns
		$\overline{\text{PL}}$ to Q; see Fig. 9 [2]						
		V _{CC} = 3.0 V			27		30	ns
		V _{CC} = 4.5 V			17		20	ns
		V _{CC} = 6.0 V			13		15	ns
t _t	transition time	Q; see Fig. 9 [3]						
		V _{CC} = 3.0 V			8		10	ns
		V _{CC} = 4.5 V			7		9	ns
		V _{CC} = 6.0 V			7		9	ns
t _w	pulse width	STCP HIGH or LOW; see Fig. 7						
		V _{CC} = 3.0 V	25			31		ns
		V _{CC} = 4.5 V	20			24		ns
		V _{CC} = 6.0 V	17			20		ns
		SHCP HIGH or LOW; see Fig. 7						
		V _{CC} = 3.0 V	25			31		ns
		V _{CC} = 4.5 V	20			24		ns
		V _{CC} = 6.0 V	17			20		ns

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Symbol	Parameter	Conditions	-40 °C to +125 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_w	pulse width	$\overline{MR}$ LOW; see Fig. 8						
		$V_{CC} = 3.0\text{ V}$	25			31		ns
		$V_{CC} = 4.5\text{ V}$	20			24		ns
		$V_{CC} = 6.0\text{ V}$	17			20		ns
		$\overline{PL}$ LOW; see Fig. 9						
		$V_{CC} = 3.0\text{ V}$	25			31		ns
		$V_{CC} = 4.5\text{ V}$	20			24		ns
		$V_{CC} = 6.0\text{ V}$	17			20		ns
t_{rec}	recovery time	$\overline{MR}$ to SHCP; see Fig. 10						
		$V_{CC} = 3.0\text{ V}$	20			23		ns
		$V_{CC} = 4.5\text{ V}$	15			18		ns
		$V_{CC} = 6.0\text{ V}$	13			15		ns
t_{su}	set-up time	Dn to STCP; see Fig. 11						
		$V_{CC} = 3.0\text{ V}$	20			23		ns
		$V_{CC} = 4.5\text{ V}$	15			18		ns
		$V_{CC} = 6.0\text{ V}$	13			15		ns
		DS to SHCP; see Fig. 11						
		$V_{CC} = 3.0\text{ V}$	20			23		ns
		$V_{CC} = 4.5\text{ V}$	15			18		ns
		$V_{CC} = 6.0\text{ V}$	13			15		ns
		$\overline{PL}$ to SHCP; see Fig. 12						
		$V_{CC} = 3.0\text{ V}$	20			23		ns
		$V_{CC} = 4.5\text{ V}$	15			18		ns
		$V_{CC} = 6.0\text{ V}$	13			15		ns
t_h	hold time	Dn to STCP; see Fig. 11						
		$V_{CC} = 3.0\text{ V}$	5			5		ns
		$V_{CC} = 4.5\text{ V}$	5			5		ns
		$V_{CC} = 6.0\text{ V}$	5			5		ns
		$\overline{PL}, DS$ to SHCP; see Fig.11						
		$V_{CC} = 3.0\text{ V}$	5			5		ns
		$V_{CC} = 4.5\text{ V}$	5			5		ns
		$V_{CC} = 6.0\text{ V}$	5			5		ns

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8-bit shift register with input flip-flops

Symbol	Parameter	Conditions	-40 °C to +125 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$f_{\max}$	maximum frequency	SHCP; see Fig. 7						
		$V_{CC} = 3.0 \text{ V}$	20			16		MHz
		$V_{CC} = 4.5 \text{ V}$	24			20		MHz
		$V_{CC} = 6.0 \text{ V}$	28			24		MHz
C_{PD}	power dissipation capacitance	$f = 1 \text{ MHz};$ $V_i = \text{GND to } V_{CC};$ [4]		26				pF
EM74HCT597								
t_{pd}	propagation delay	SHCP to Q; see Fig. 7 [2]						
		$V_{CC} = 4.5 \text{ V}$			17		20	ns
		$\overline{MR}$ to Q; see Fig. 8 [2]						
		$V_{CC} = 4.5 \text{ V}$			17		20	ns
		STCP to Q; see Fig. 7 [2]						
		$V_{CC} = 4.5 \text{ V}$			17		20	ns
		$\overline{PL}$ to Q; see Fig. 9 [2]						
t_t	transition time	$V_{CC} = 4.5 \text{ V}$			17		20	ns
		Q; see Fig. 9 [3]						
t_w	pulse width	$V_{CC} = 4.5 \text{ V}$			7		9	ns
		STCP HIGH or LOW; see Fig. 7						
		$V_{CC} = 4.5 \text{ V}$	20			24		ns
		SHCP HIGH or LOW; see Fig. 7						
		$V_{CC} = 4.5 \text{ V}$	15			18		ns
		$\overline{MR}$ LOW; see Fig. 8						
		$V_{CC} = 4.5 \text{ V}$	31			38		ns
t_{rec}	recovery time	$\overline{PL}$ LOW; see Fig. 9						
		$V_{CC} = 4.5 \text{ V}$	25			30		ns
t_{su}	set-up time	$\overline{MR}$ to SHCP; see Fig. 10						
		$V_{CC} = 4.5 \text{ V}$	15			18		ns
		Dn to STCP; see Fig. 11						
		$V_{CC} = 4.5 \text{ V}$	15			18		ns
		DS to SHCP; see Fig. 11						
		$V_{CC} = 4.5 \text{ V}$	15			18		ns
		$\overline{PL}$ to SHCP; see Fig. 12						
		$V_{CC} = 4.5 \text{ V}$	15			18		ns

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Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_h	hold time	Dn to STCP; see Fig. 11						
		$V_{CC} = 4.5 \text{ V}$	5			5		ns
		$\overline{PL}, DS$ to SHCP; see Fig.11						
		$V_{CC} = 4.5 \text{ V}$	5			5		ns
f_{max}	maximum frequency	SHCP; see Fig. 7						
		$V_{CC} = 4.5 \text{ V}$	24			20		MHz
C_{PD}	power dissipation capacitance	$f = 1 \text{ MHz};$ $V_I = \text{GND to } V_{CC};$ [4]		28				pF

[1] Typical values are measured at $T_{amb} = 25 \text{ °C}$.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] t_t is the same as t_{THL} and t_{TLH} .

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

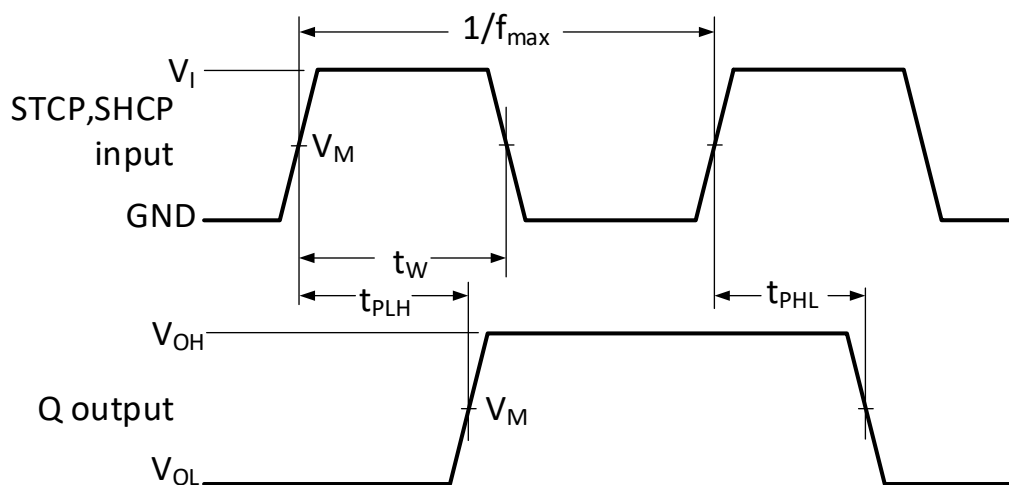
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

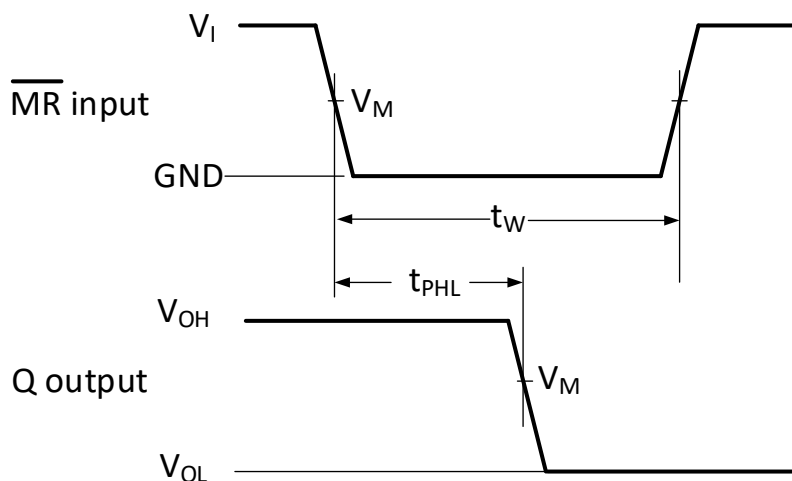
11. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. SHCP and STCP clock inputs to Q output propagation delays, pulse width and maximum clock frequency



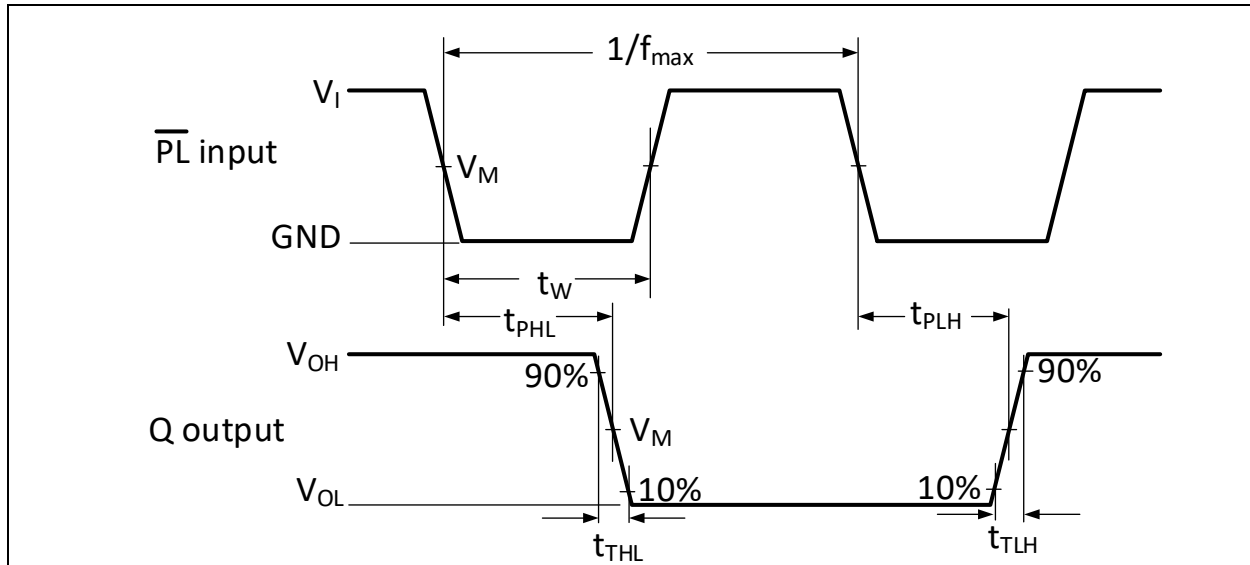
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 8. Input $\overline{MR}$ to Q output propagation delays and $\overline{MR}$ pulse width

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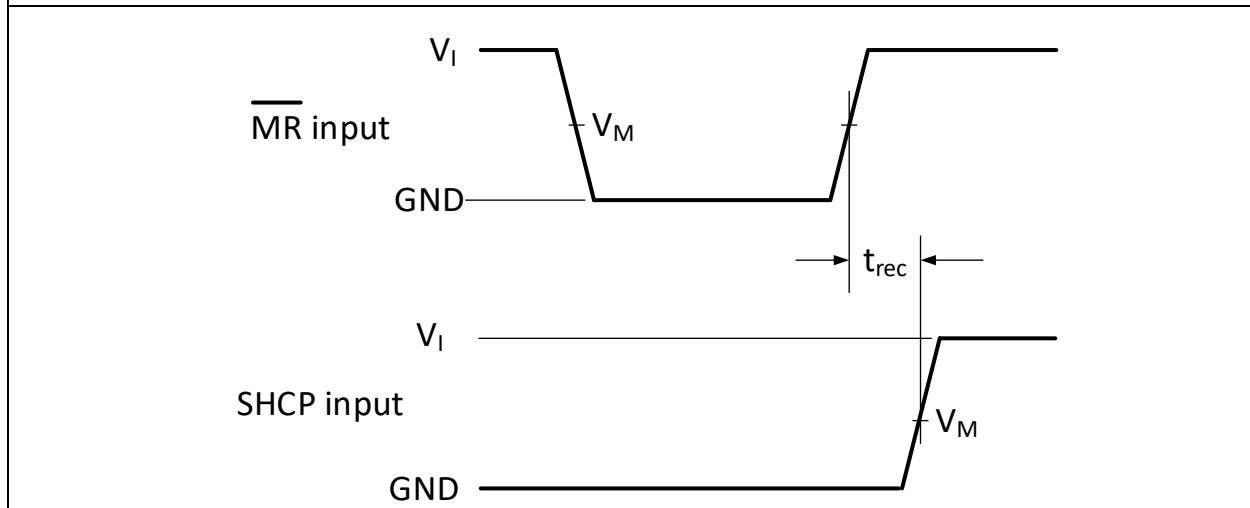
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Measurement points are given in Table 8.

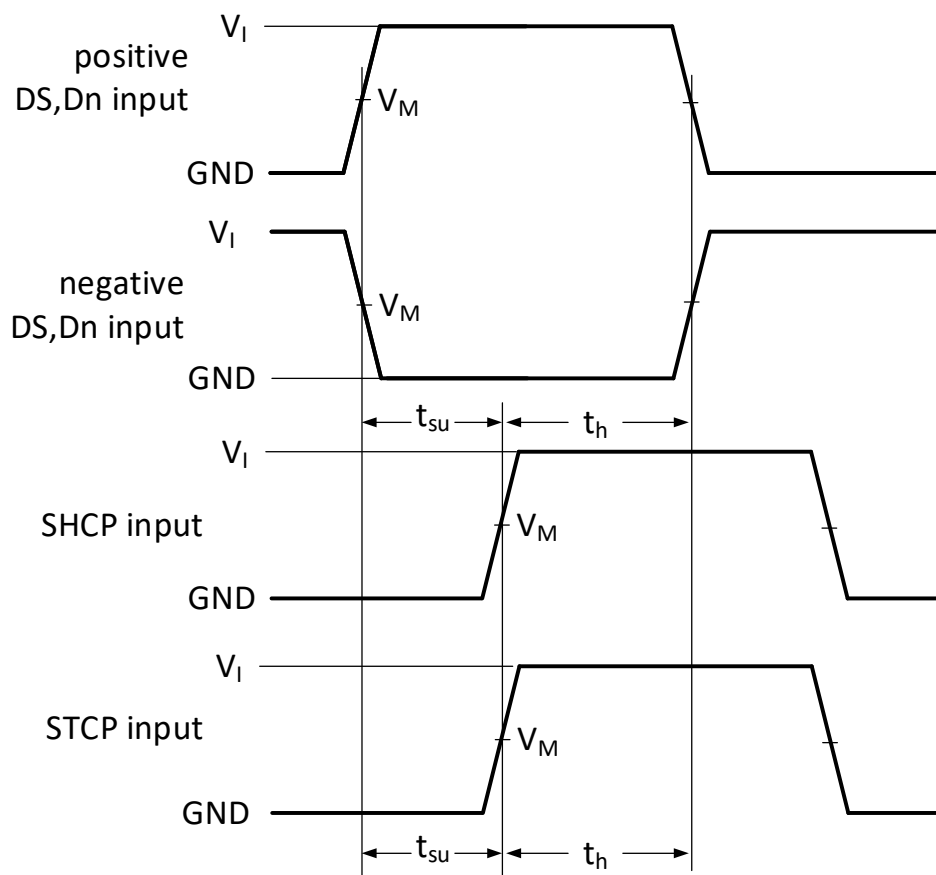
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 9. Input $\overline{PL}$ to Q output propagation delays, $\overline{PL}$ pulse width and output transition times



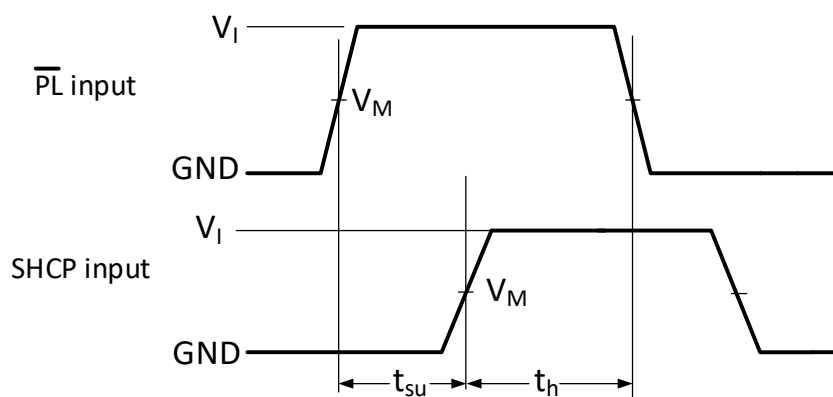
Measurement points are given in Table 8.

Fig. 10. Input $\overline{MR}$ to shift clock SHCP and storage clock STCP recovery times



Measurement points are given in Table 8.

Fig. 11. Set-up and hold times for DS, Dn inputs to SHCP, STCP inputs



Measurement points are given in Table 8.

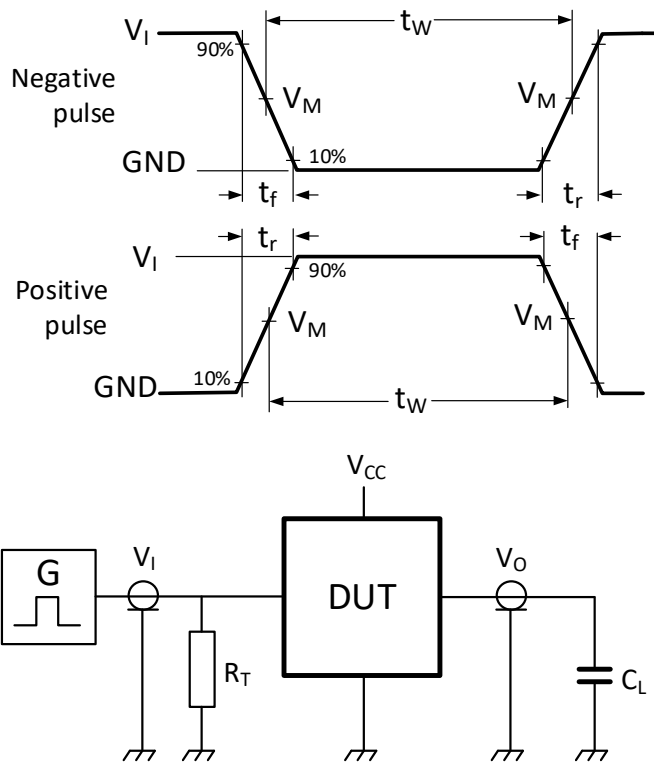
Fig. 12. Set-up and hold times for $\overline{PL}$ input to SHCP input

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Table 8. Measurement points

Type	Input		Output
	V_M	V_I	V_M
EM74HC597	$0.5V_{CC}$	GND to V_{CC}	$0.5V_{CC}$
EM74HCT597	1.3 V	GND to 3 V	1.3 V



Test data is given in Table 9.

Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

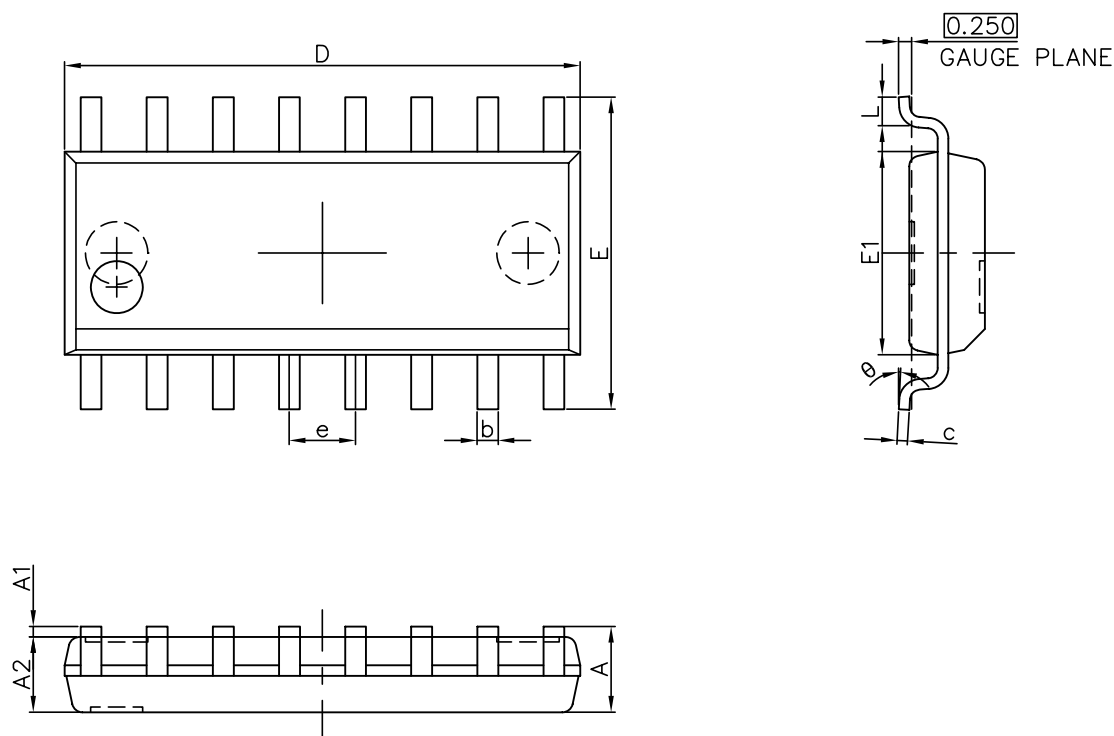
Fig. 13. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	$t_r = t_f$	C_L	
EM74HC597	V_{CC}	2.5 ns	50 pF	t_{PHL}, t_{PLH}
EM74HCT597	3 V	2.5 ns	50 pF	t_{PHL}, t_{PLH}

12. Package Outline

SOP-16L

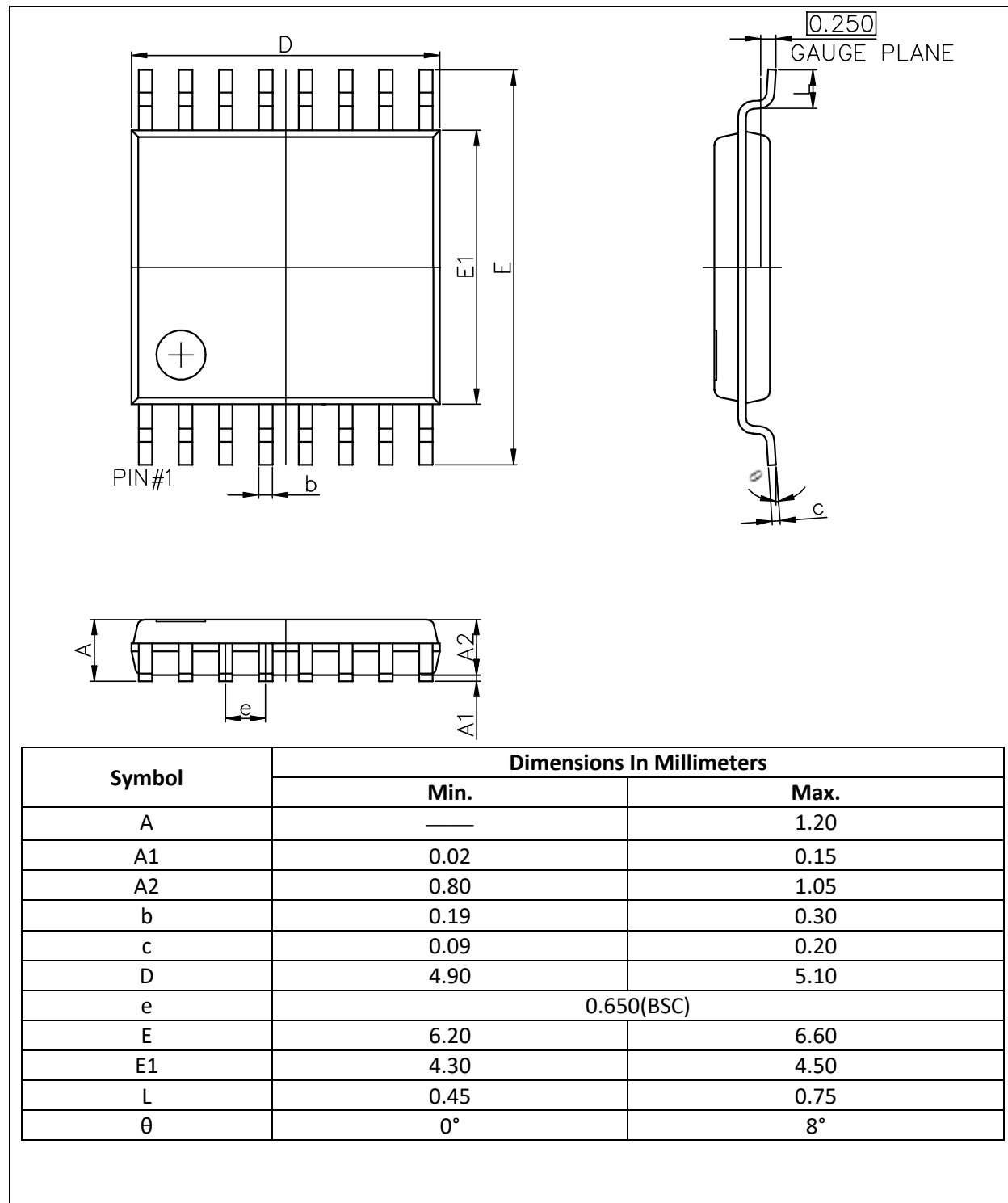


Symbol	Dimensions In Millimeters	
	Min.	Max.
A	—	1.75
A1	0.05	0.25
A2	1.30	1.60
b	0.33	0.51
c	0.17	0.25
D	9.80	10.00
e	1.27(BSC)	
E	5.80	6.20
E1	3.80	4.00
L	0.40	1.27
θ	0°	8°

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8-bit shift register with input flip-flops

TSSOP-16L



13. Tape and Reel Information

13.1. Carrier tape dimensions

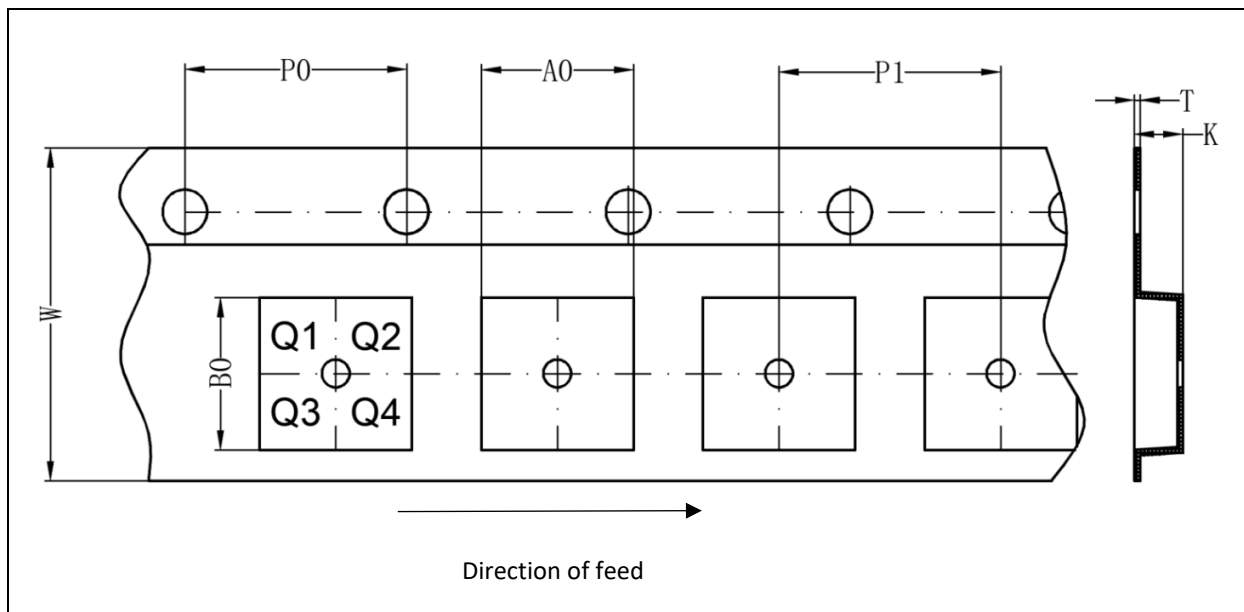


Table 10. Carrier tape dimensions

Package version	A0(mm)	B0(mm)	K0(mm)	T(mm)	P1(mm)	W(mm)	P0(mm)	PIN 1
SOP-16L	6.5	10.45	2.1	0.22	8	16	4	Q1
TSSOP-16L	6.7	5.45	1.6	0.25	8	12	4	Q1

13.2. Reel and box dimensions

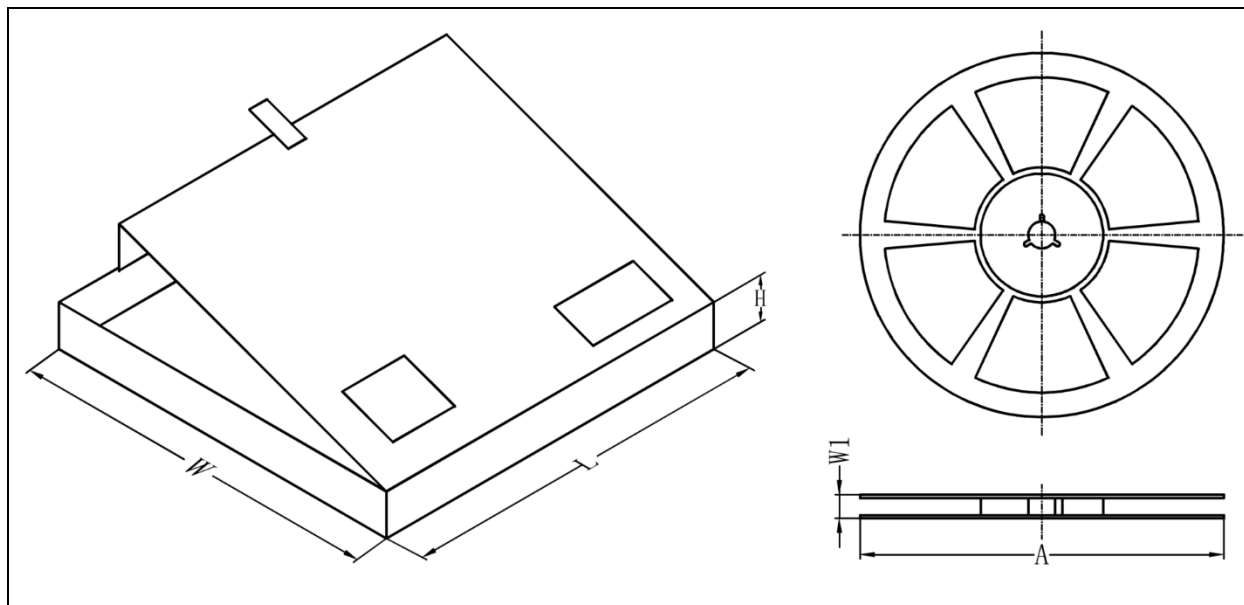


Table 11. Dimensions and quantities

Package version	Type NO. ending	Reel Dimension A (mm)	Reel Width W1 (mm)	SPQ (pcs) [1]	Reels per box	Outer box dimensions L×W×H(mm) [2]
SOP-16L	D	330	22.4	3000	1	358x340x50
TSSOP-16L	PW	330	18.4	3000	1	358x340x50

[1] Packing quantity dependent on specific product type. Please contact your local Energymath representative for ordering.

[2] Dimensions for reference only.

14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
TTL	Transistor-Transistor Logic
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model

15. Revision History

Table 13. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
EM74HC_HCT597 Rev. 1.1	Mar 20, 2026	Product datasheet		EM74HC_HCT597 Rev. 1.0
Modifications:	• Section 12: Package outline updated. • Section 13: Added tape and reel information.			
EM74HC_HCT597 Rev. 1.0	Nov 29, 2024	Product datasheet		